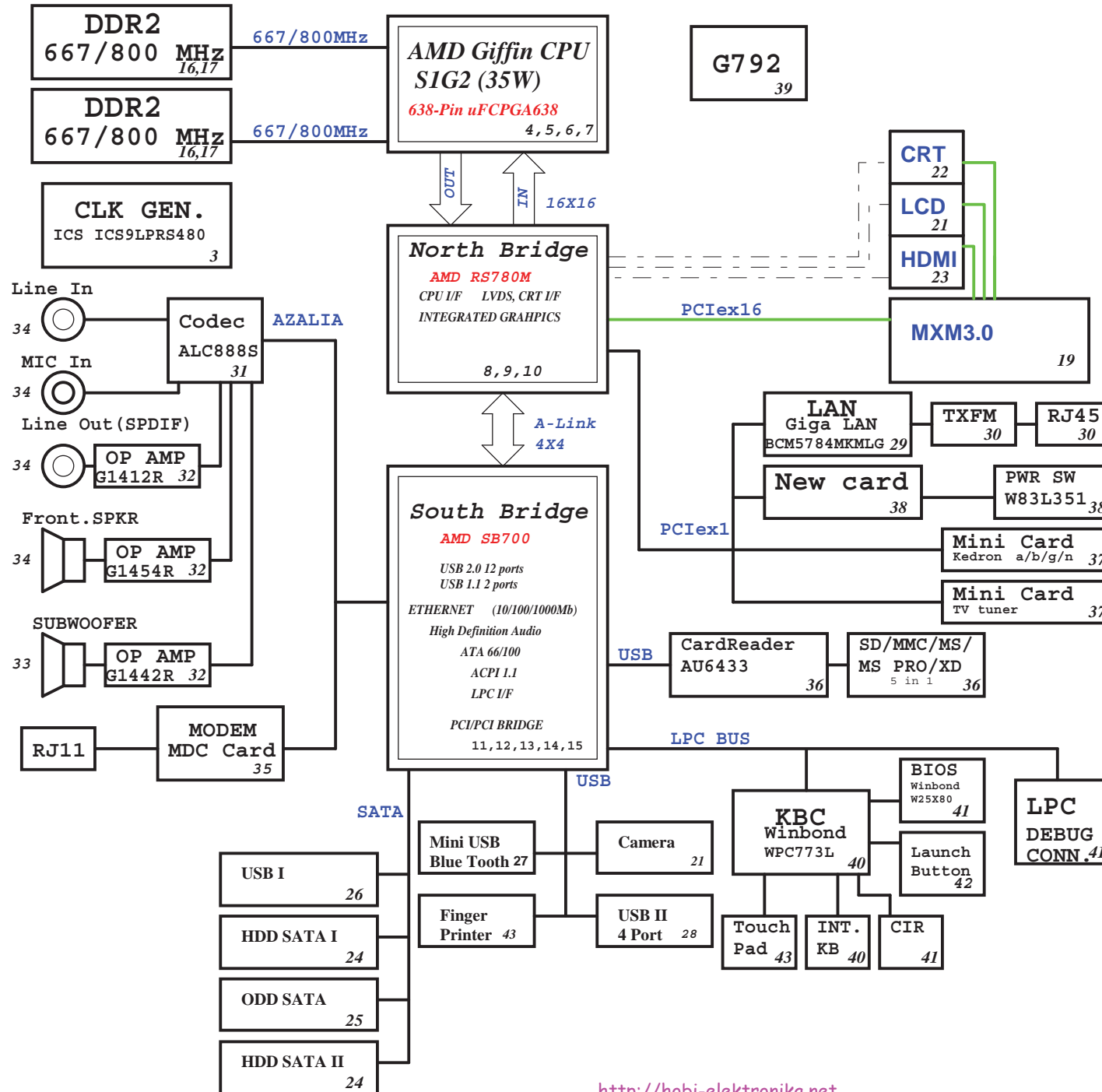


JM70-PU (AS 17") Block Diagram

Project code: 91.4CE01.001
PCB P/N : 48.4CE01.0SC
REVISION : 08255-SC



PCB STACKUP

TOP _____

VCC _____

S _____

S _____

GND _____

BOTTOM _____

SYSTEM DC/DC TPS51125 49	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (7A)
	3D3V_S5 (7A)
SYSTEM DC/DC TPS51124 50	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (8A)
	1D2V_S0 (5A)
SYSTEM DC/DC TPS51117 52	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 (10A)
RT9026PFP 51	
1D8V_S3	DDR_VREF_S3
	0D9V_S3 (1A)
RT9166 51	
3D3V_S0	2D5V_S0 (300mA)
G957 51	
3D3V_S0	1D5V_S0 (1A)
G9161 (UMA) 51	
3D3V_S5	1D2V_S5 (400mA)
G9131 (DIS) 51	
3D3V_S5	1D2V_S5 (300mA)
CHARGER MAX8731A 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC ISL6265HR 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0
	0~1.55V 18A
	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

BLOCK DIAGRAM		
Size A3	Document Number	Rev
	JM70-PU	-2
Date: Monday, March 02, 2009	Sheet 1 of 56	

5	4	3	2	1
D				
C				
B				
A				

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size

A3

Document Number

JM70-PU

Rev

-2

Date:

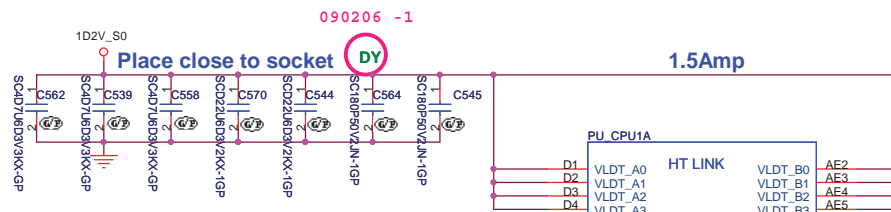
Monday, March 02, 2009

Sheet

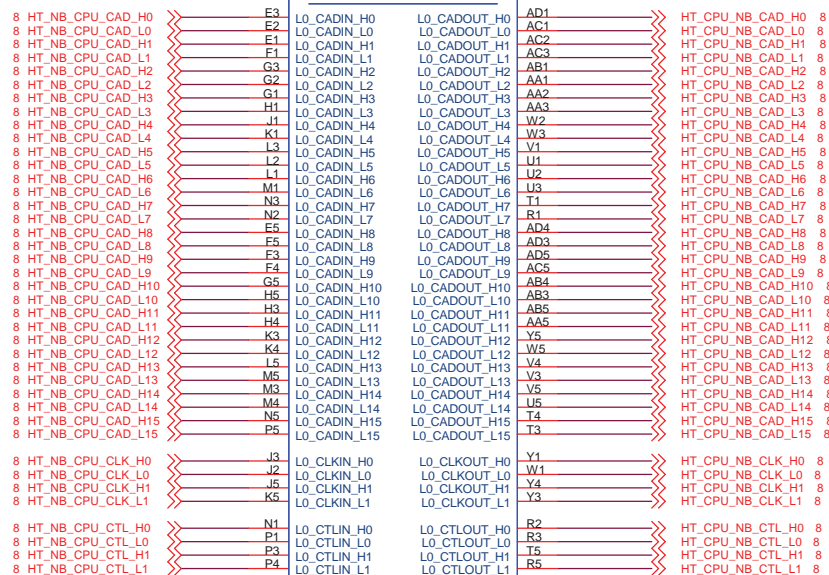
2

of

56



State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V



SKT-CPU638P-GP.U2

62 10055 111
ZND = 62.10055.251

090109 SC

SKT-BGA638H176

<Core Design>

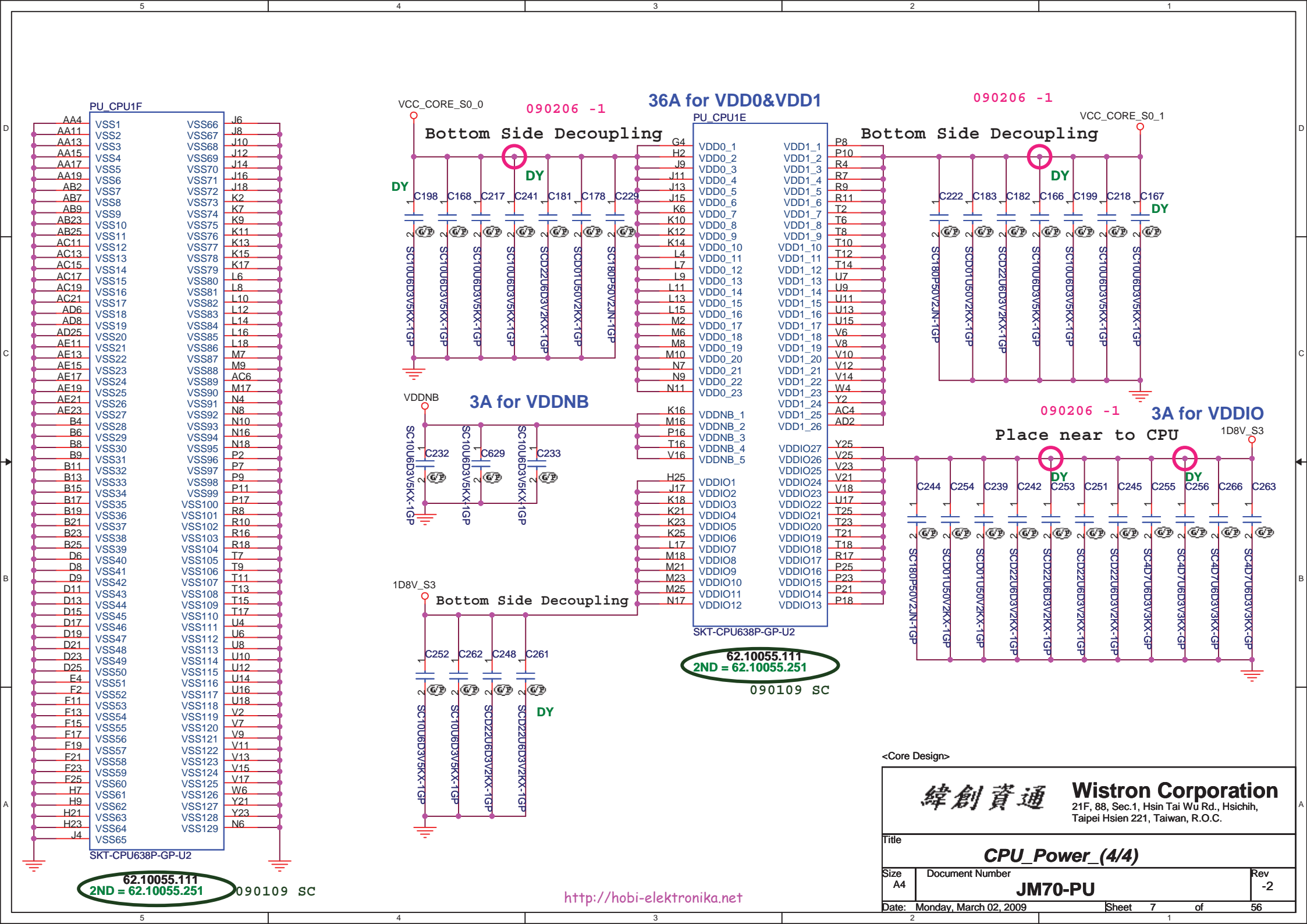
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

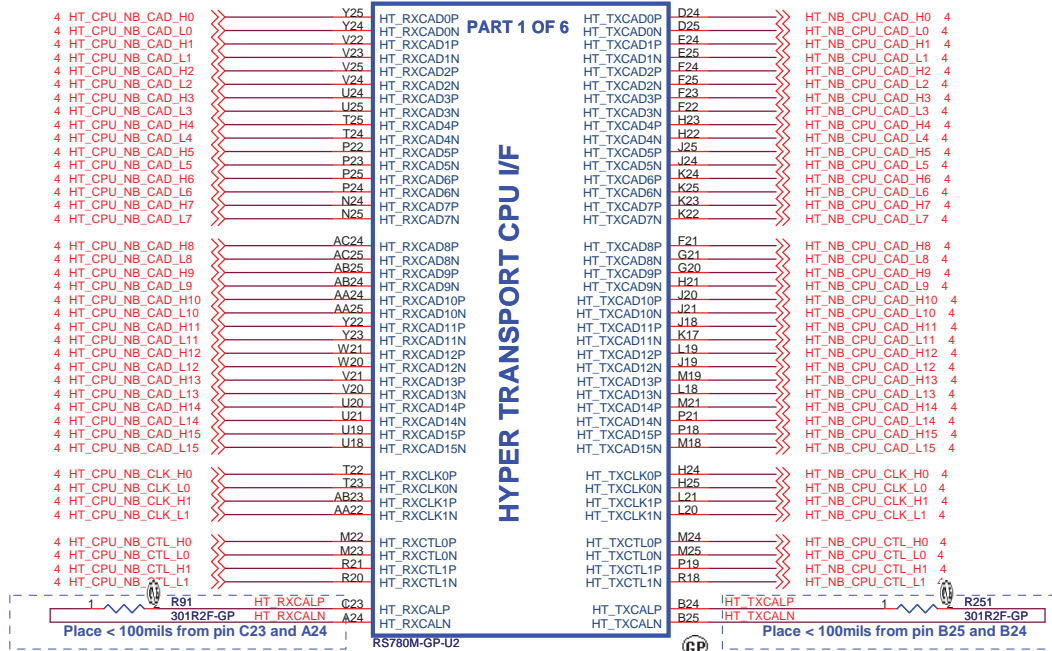
Title			CPU_HT_LINK I/F (1/4)		
Size	Document Number				Rev
A3	JM70-PU				-2
Date:	Friday, March 06, 2009				Sheet 4 of 56

— — — |

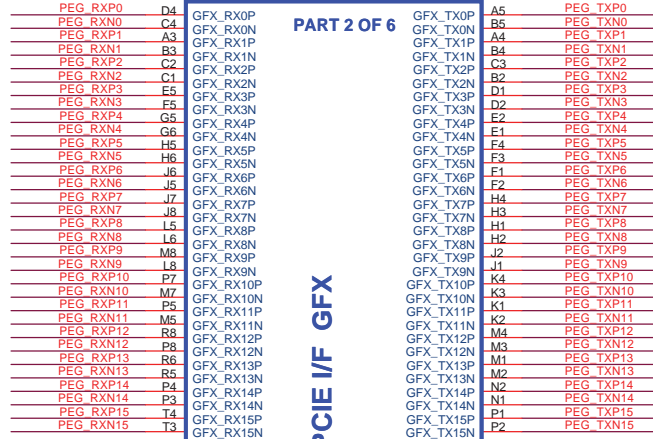


<http://hobi-elektronika.net>





PU_NB1B



19 PEG_RXN[15.0] >>>
19 PEG_RXP[15.0] >>>

LAN
MINICARD
MINICARD TV
NEW CARD

A-LINK

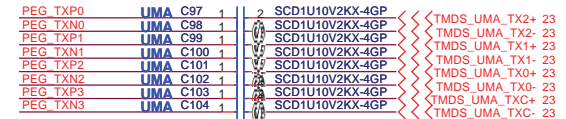
TPAD14-GP53
TPAD14-GP52

11 ALINK_NBRX_SBTX_P0
11 ALINK_NBRX_SBTX_N0
11 ALINK_NBRX_SBTX_P1
11 ALINK_NBRX_SBTX_N1
11 ALINK_NBRX_SBTX_P2
11 ALINK_NBRX_SBTX_N2
11 ALINK_NBRX_SBTX_P3
11 ALINK_NBRX_SBTX_N3

RS780M-GP-U2



http://hobi-elektronika.net



RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

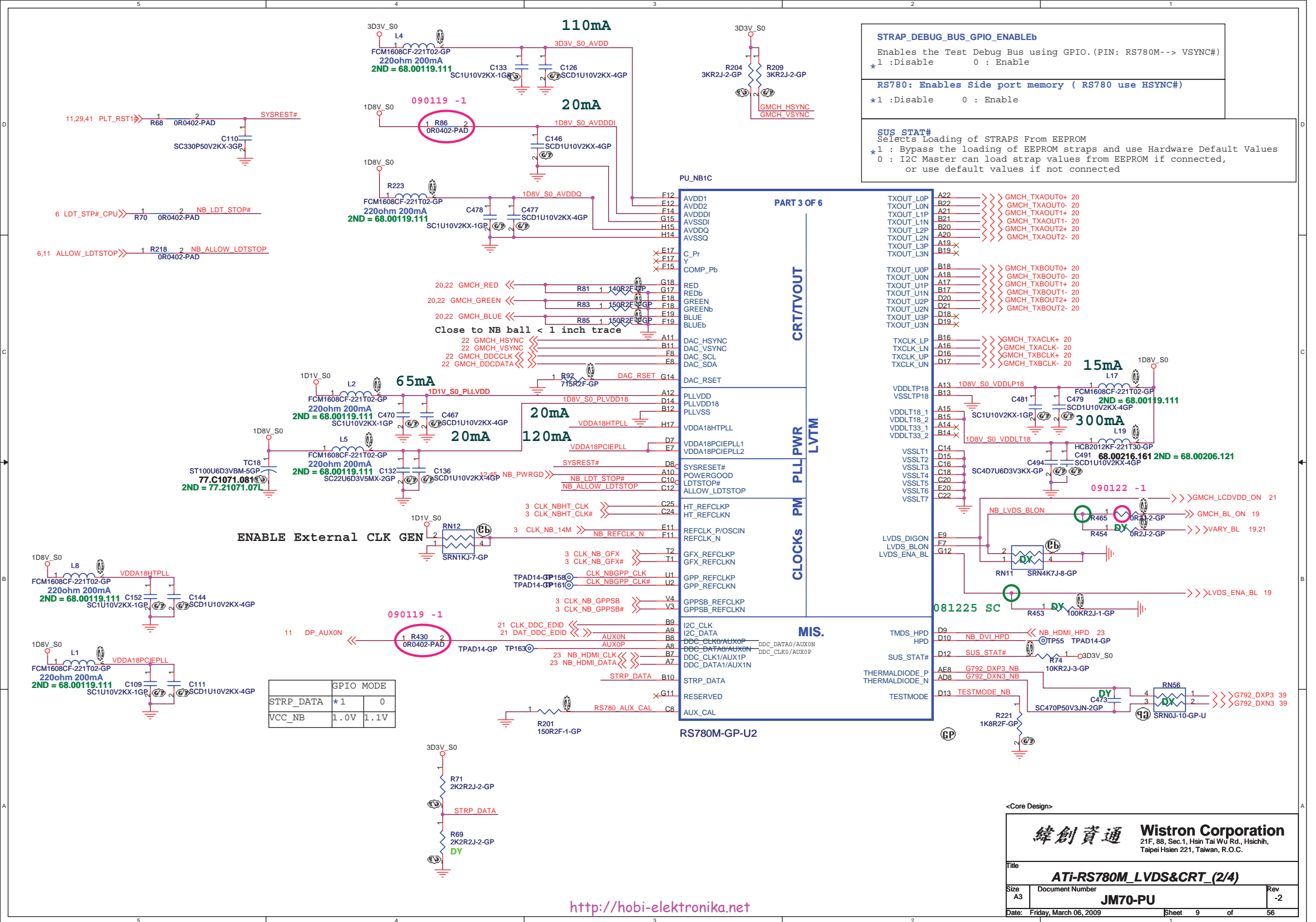
PCIE As SW request 11/17
Port 1 => Onboard LAN
Port 2 => Mini Card WLAN
Port 3 => Mini Card#2
Port 4 => New Card
Port 5,6 => NC

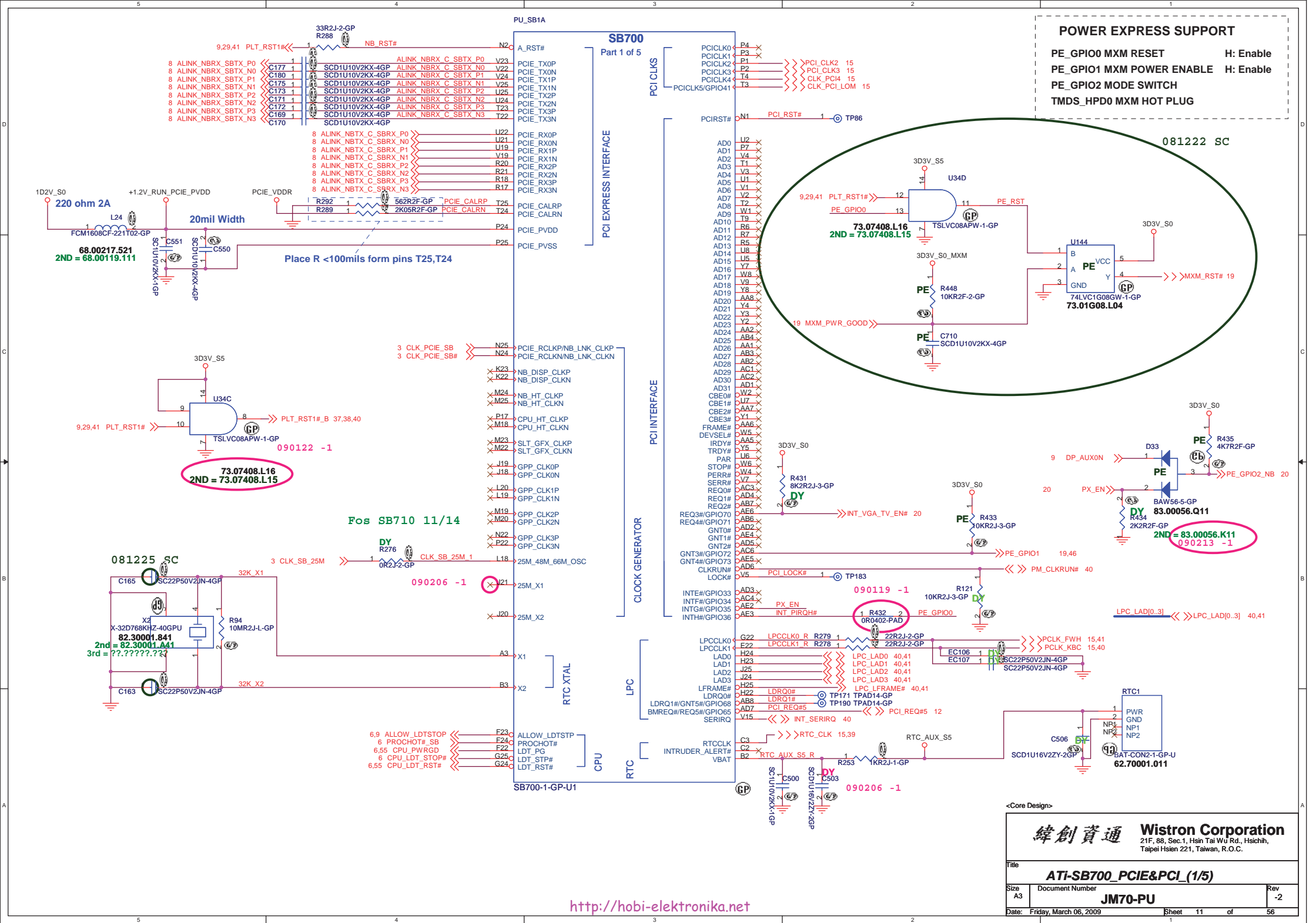
LAN
MINICARD
MINICARD TV
NEW CARD

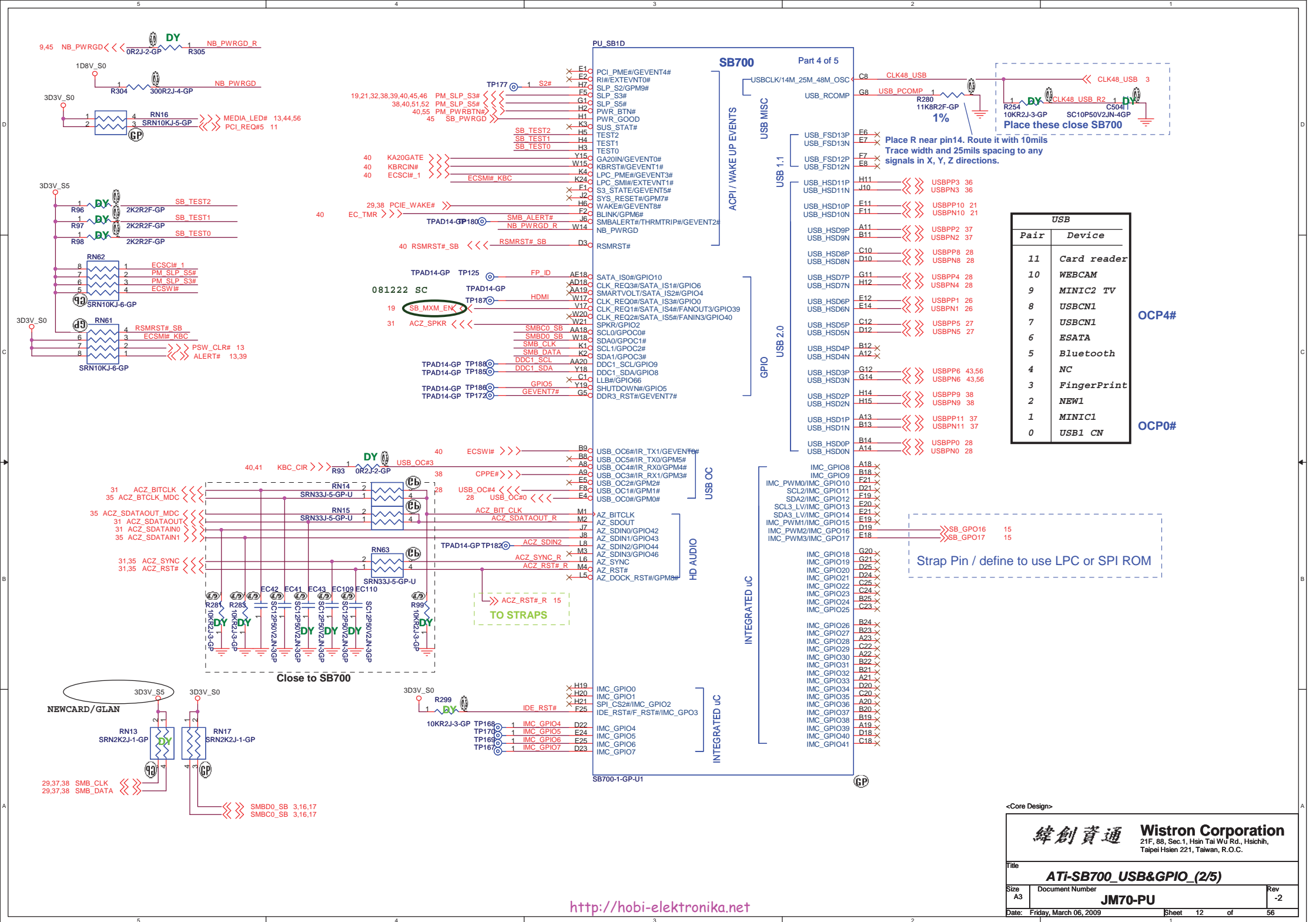
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

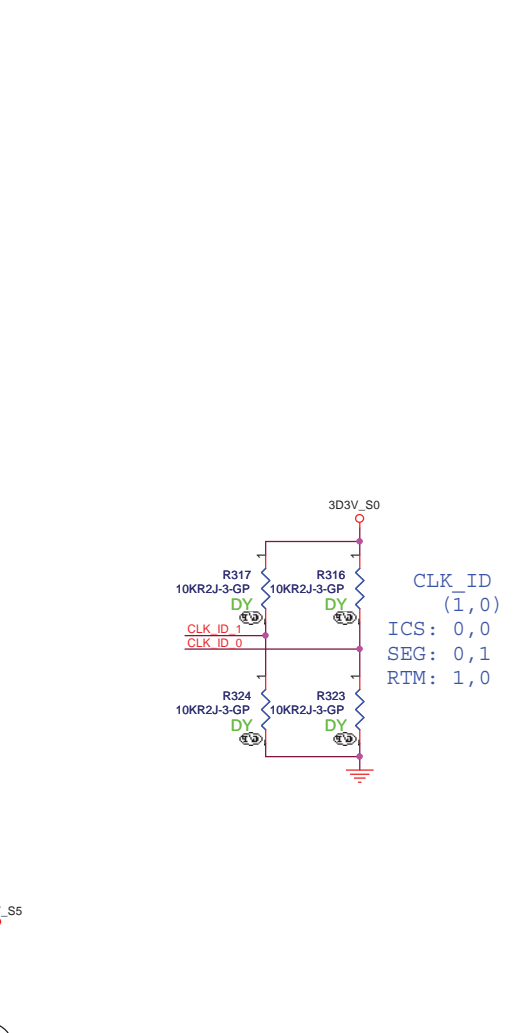
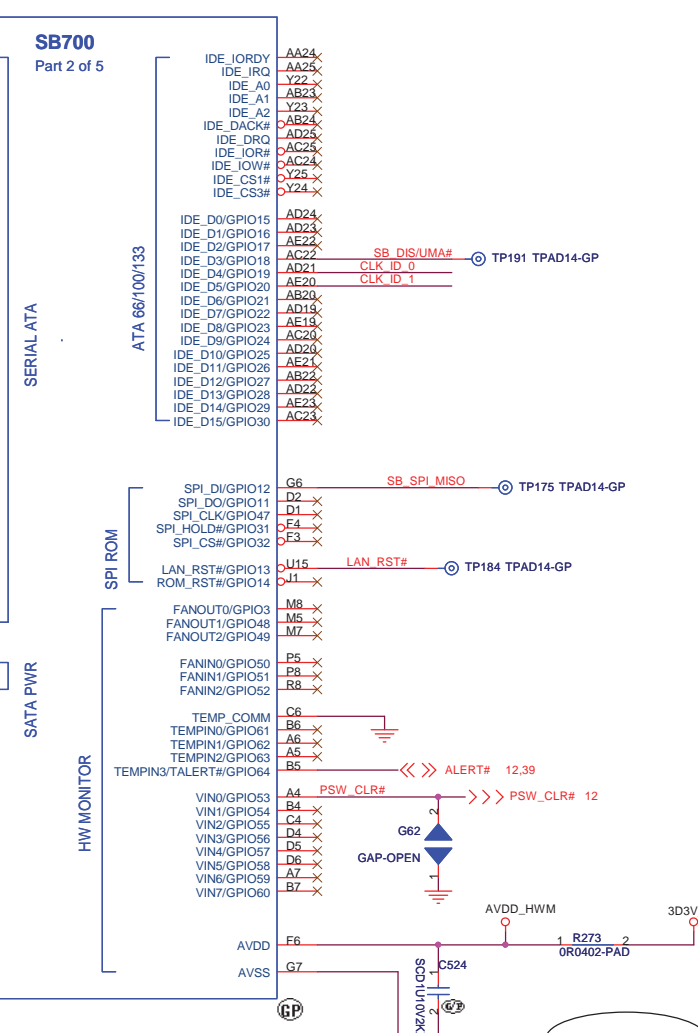
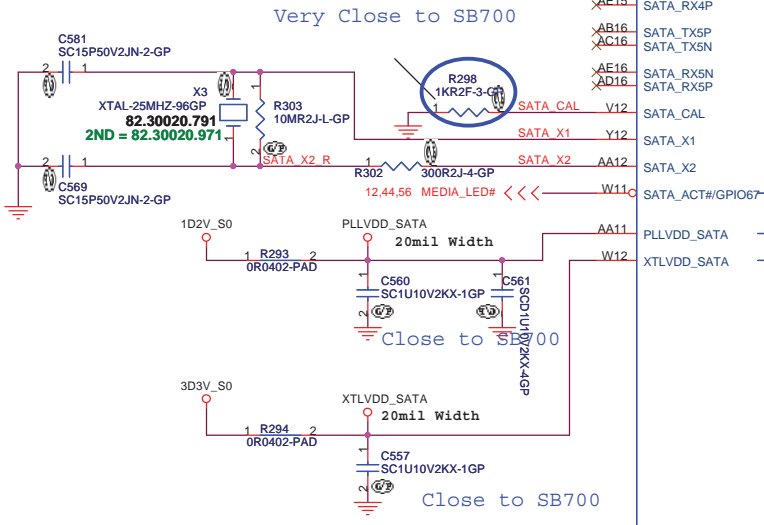
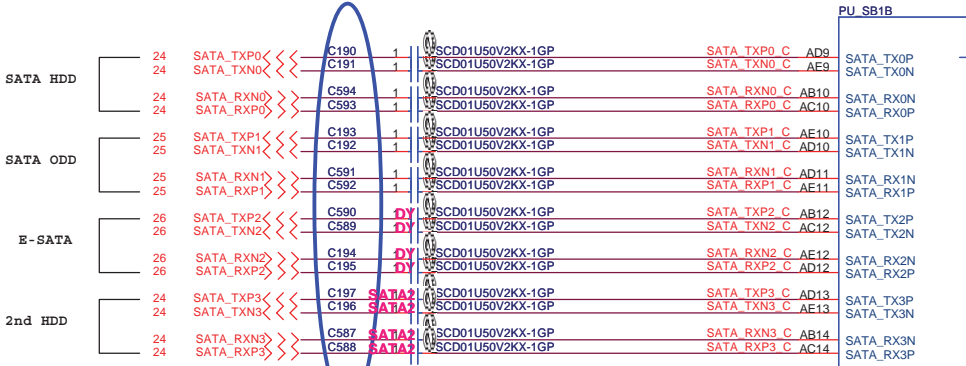
Title	ATI-RS780M_HT LINK&PCIE(1/3)	Rev	-2
Size	A3	Document Number	JM70-PU
Date	Friday, March 06, 2009	Sheet	8 of 56





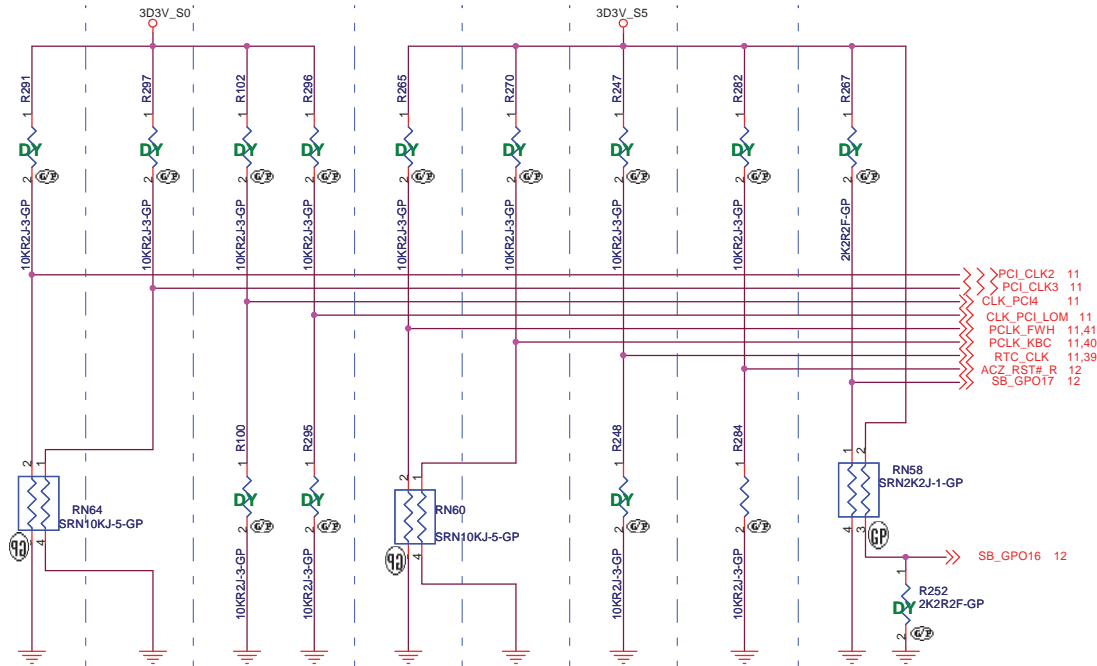


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]



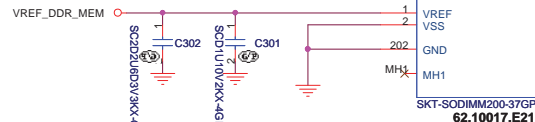
5,18 MEM_MB_ADD0 >> 102 A0
5,18 MEM_MB_ADD1 >> 101 A1
5,18 MEM_MB_ADD2 >> 100 A2
5,18 MEM_MB_ADD3 >> 98 A3
5,18 MEM_MB_ADD4 >> 94 A4
5,18 MEM_MB_ADD5 >> 97 A5
5,18 MEM_MB_ADD6 >> 92 A6
5,18 MEM_MB_ADD7 >> 93 A7
5,18 MEM_MB_ADD8 >> 90 A8
5,18 MEM_MB_ADD9 >> 91 A9
5,18 MEM_MB_ADD10 >> 105 A10/AP
5,18 MEM_MB_ADD11 >> 90 A11
5,18 MEM_MB_ADD12 >> 116 A12
5,18 MEM_MB_ADD13 >> 86 A13
5,18 MEM_MB_ADD14 >> 84 A14
5,18 MEM_MB_ADD15 >> 85 A15
5,18 MEM_MB_BANK2 >> A16/BA2
5,18 MEM_MB_BANK0 >> 107 BA0
5,18 MEM_MB_BANK1 >> 106 BA1

5 MEM_MB_DATA0 >> 5 DQ0
5 MEM_MB_DATA1 >> 7 DQ1
5 MEM_MB_DATA2 >> 17 DQ2
5 MEM_MB_DATA3 >> 19 DQ3
5 MEM_MB_DATA4 >> 4 DQ4
5 MEM_MB_DATA5 >> 6 DQ5
5 MEM_MB_DATA6 >> 14 DQ6
5 MEM_MB_DATA7 >> 16 DQ7
5 MEM_MB_DATA8 >> 23 DQ8
5 MEM_MB_DATA9 >> 25 DQ9
5 MEM_MB_DATA10 >> 35 DQ10
5 MEM_MB_DATA11 >> 37 DQ11
5 MEM_MB_DATA12 >> 20 DQ12
5 MEM_MB_DATA13 >> 22 DQ13
5 MEM_MB_DATA14 >> 36 DQ14
5 MEM_MB_DATA15 >> 38 DQ15
5 MEM_MB_DATA16 >> 43 DQ16
5 MEM_MB_DATA17 >> 45 DQ17
5 MEM_MB_DATA18 >> 55 DQ18
5 MEM_MB_DATA19 >> 57 DQ19
5 MEM_MB_DATA20 >> 44 DQ20
5 MEM_MB_DATA21 >> 46 DQ21
5 MEM_MB_DATA22 >> 58 DQ22
5 MEM_MB_DATA23 >> 61 DQ23
5 MEM_MB_DATA24 >> 63 DQ24
5 MEM_MB_DATA25 >> 73 DQ25
5 MEM_MB_DATA26 >> 75 DQ26
5 MEM_MB_DATA27 >> 62 DQ27
5 MEM_MB_DATA28 >> 64 DQ28
5 MEM_MB_DATA29 >> 74 DQ29
5 MEM_MB_DATA30 >> 76 DQ30
5 MEM_MB_DATA31 >> 123 DQ31
5 MEM_MB_DATA32 >> 125 DQ32
5 MEM_MB_DATA33 >> 135 DQ33
5 MEM_MB_DATA34 >> 137 DQ34
5 MEM_MB_DATA35 >> 124 DQ35
5 MEM_MB_DATA36 >> 126 DQ36
5 MEM_MB_DATA37 >> 134 DQ37
5 MEM_MB_DATA38 >> 136 DQ38
5 MEM_MB_DATA39 >> 141 DQ39
5 MEM_MB_DATA40 >> 143 DQ40
5 MEM_MB_DATA41 >> 151 DQ41
5 MEM_MB_DATA42 >> 153 DQ42
5 MEM_MB_DATA43 >> 140 DQ43
5 MEM_MB_DATA44 >> 142 DQ44
5 MEM_MB_DATA45 >> 152 DQ45
5 MEM_MB_DATA46 >> 154 DQ46
5 MEM_MB_DATA47 >> 157 DQ47
5 MEM_MB_DATA48 >> 159 DQ48
5 MEM_MB_DATA49 >> 173 DQ49
5 MEM_MB_DATA50 >> 175 DQ50
5 MEM_MB_DATA51 >> 158 DQ51
5 MEM_MB_DATA52 >> 160 DQ52
5 MEM_MB_DATA53 >> 174 DQ53
5 MEM_MB_DATA54 >> 176 DQ54
5 MEM_MB_DATA55 >> 179 DQ55
5 MEM_MB_DATA56 >> 181 DQ56
5 MEM_MB_DATA57 >> 188 DQ57
5 MEM_MB_DATA58 >> 191 DQ58
5 MEM_MB_DATA59 >> 180 DQ59
5 MEM_MB_DATA60 >> 182 DQ60
5 MEM_MB_DATA61 >> 192 DQ61
5 MEM_MB_DATA62 >> 194 DQ62
5 MEM_MB_DATA63 >> 194 DQ63

5 MEM_MB_DQS0_N >> 11 DQS0#
5 MEM_MB_DQS1_N >> 29 DQS1#
5 MEM_MB_DQS2_N >> 49 DQS2#
5 MEM_MB_DQS3_N >> 68 DQS3#
5 MEM_MB_DQS4_N >> 129 DQS4#
5 MEM_MB_DQS5_N >> 146 DQS5#
5 MEM_MB_DQS6_N >> 167 DQS6#
5 MEM_MB_DQS7_N >> 186 DQS7#

5 MEM_MB_DQS0_P >> 13 DQS0#
5 MEM_MB_DQS1_P >> 31 DQS1#
5 MEM_MB_DQS2_P >> 51 DQS2#
5 MEM_MB_DQS3_P >> 70 DQS3#
5 MEM_MB_DQS4_P >> 131 DQS4#
5 MEM_MB_DQS5_P >> 148 DQS5#
5 MEM_MB_DQS6_P >> 169 DQS6#
5 MEM_MB_DQS7_P >> 188 DQS7#

5,18 MEM_MB0_ODT0 >> 114 OTD0
5,18 MEM_MB0_ODT1 >> 119 OTD1



Place C2.2uF and 0.1uF < 500mils from DDR connector

HI 9.2mm

62.10017.E21

081225 SC

ZND = 62.10017.071

<http://hobi-elektronika.net>

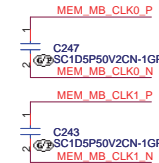
NORMAL TYPE

PU DM2
RAS# >> 108 A0
WE# >> 109 A1
CAS# >> 113 A2
CS0# >> 110 A3
CS1# >> 115 A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
A16/BA2
BA0
BA1
DM0 >> 10 MEM_MB_DM0 5
DM1 >> 26 MEM_MB_DM1 5
DM2 >> 52 MEM_MB_DM2 5
DM3 >> 67 MEM_MB_DM3 5
DM4 >> 130 MEM_MB_DM4 5
DM5 >> 147 MEM_MB_DM5 5
DM6 >> 170 MEM_MB_DM6 5
DM7 >> 185 MEM_MB_DM7 5

SDA >> 195 SMBD0_SB 3,12,16
SCL >> 197 SMBD0_SB 3,12,16
VDDSPD >> 199
SA0 >> 198
SA1 >> 200
NC#50 >> 50 X
NC#69 >> 69 X
NC#83 >> 83 X
NC#120 >> 120 X
NC#163/TEST >> 163 X
1D8V_S3 >> 81
VDD >> 82
VDD >> 87
VDD >> 88
VDD >> 95
VDD >> 96
VDD >> 103
VDD >> 104
VDD >> 111
VDD >> 112
VDD >> 117
VDD >> 118
VSS >> 3
VSS >> 8
VSS >> 9
VSS >> 12
VSS >> 15
VSS >> 18
VSS >> 21
VSS >> 24
VSS >> 27
VSS >> 28
VSS >> 33
VSS >> 34
VSS >> 38
VSS >> 40
VSS >> 41
VSS >> 42
VSS >> 47
VSS >> 48
VSS >> 53
VSS >> 54
VSS >> 59
VSS >> 60
VSS >> 65
VSS >> 66
VSS >> 71
VSS >> 72
VSS >> 77
VSS >> 78
VSS >> 121
VSS >> 122
VSS >> 127
VSS >> 128
VSS >> 132
VSS >> 133
VSS >> 138
VSS >> 139
VSS >> 144
VSS >> 145
VSS >> 149
VSS >> 150
VSS >> 155
VSS >> 156
VSS >> 161
VSS >> 162
VSS >> 165
VSS >> 168
VSS >> 171
VSS >> 172
VSS >> 177
VSS >> 178
VSS >> 183
VSS >> 184
VSS >> 187
VSS >> 190
VSS >> 193
VSS >> 196
GND >> 201
MH2 >> GP

(A2)

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



<Core Design>

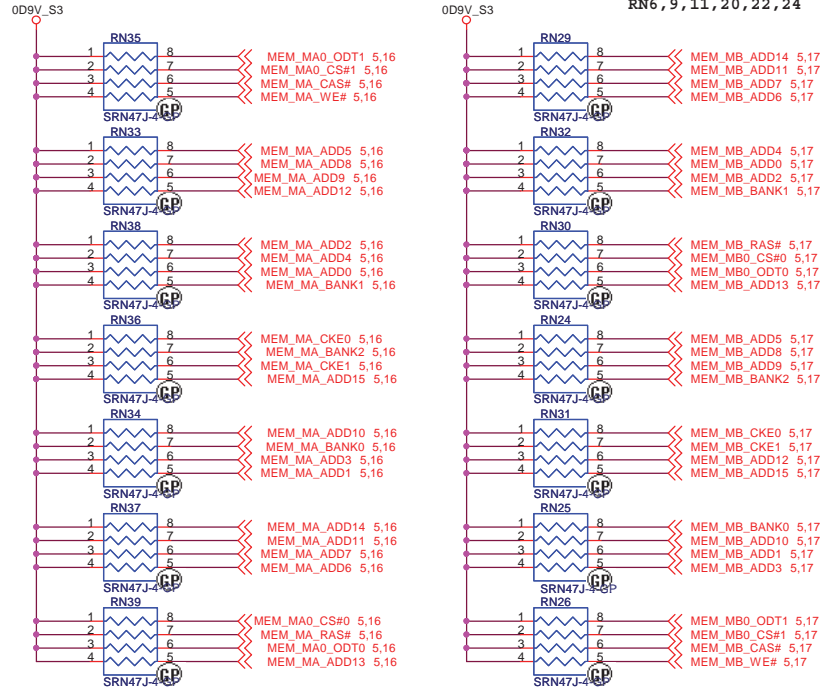
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		DDR_SO-DIMM SKT_2	
Size	Document Number	JM70-PU	
Custom		Rev -2	
Date:	Friday, March 06, 2009	Sheet 17	of 56

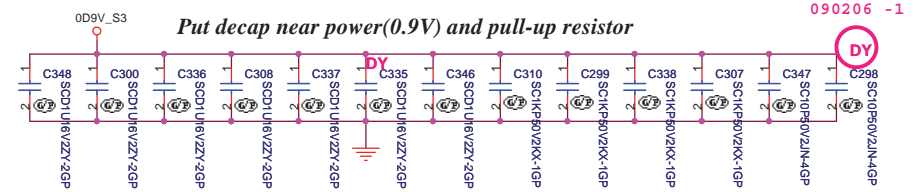
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

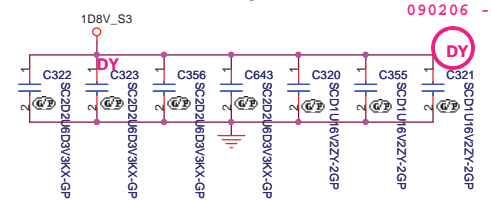
Net swap 11/14
RN6,9,11,20,22,24



Decoupling Capacitor

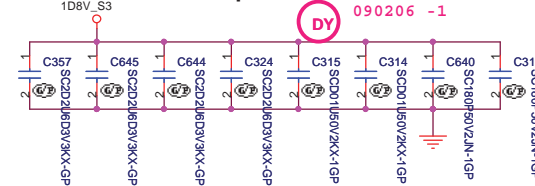


Place these Caps near DM1

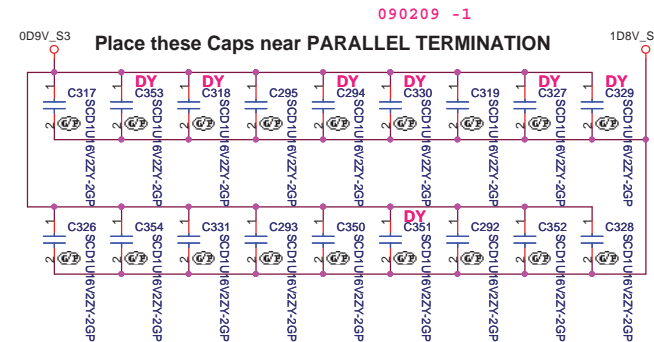


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V_S3



Place these Caps near PARALLEL TERMINATION

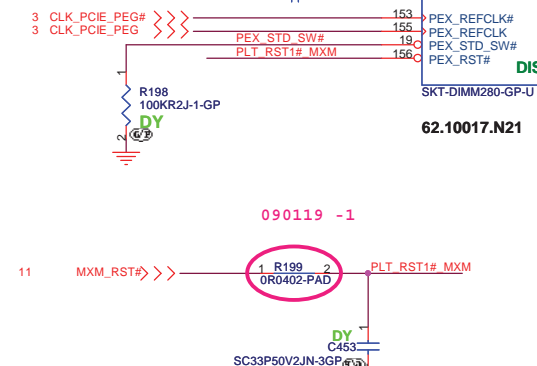
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

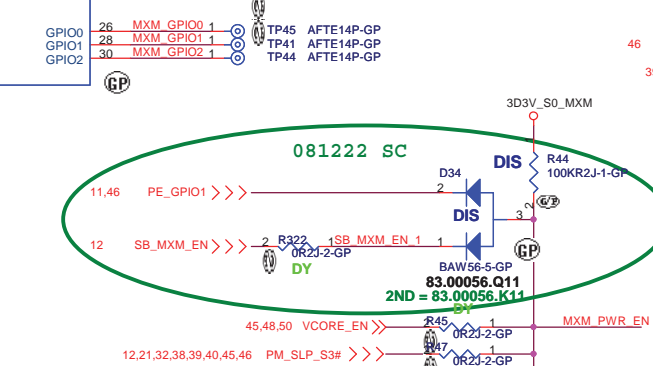
Title		
DDR DAMPING & TERMINATION		
Size	Document Number	Rev
A3	JM70-PU	-2
Date:	Friday, March 06, 2009	Sheet 18 of 56

8 PEG_TXP[15..0] << >>
8 PEG_TXN[15..0] << >>
8 PEG_RXP[15..0] << >>
8 PEG_RXN[15..0] << >>

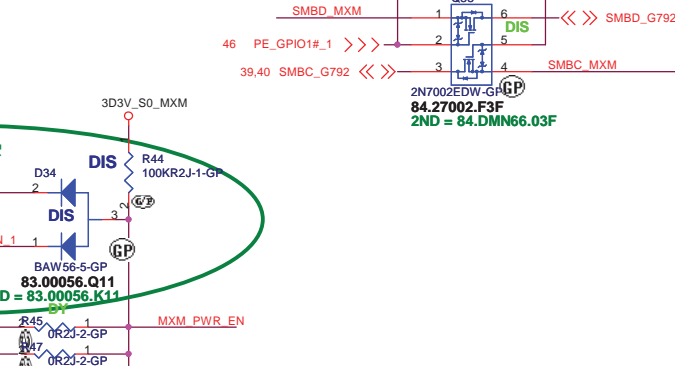
PEG_RXP0	SCD1U10V2KX-5GP	C442	DIS	GRXP0	149	PEX_RX0	277
PEG_RXN0	SCD1U10V2KX-5GP	C441	DIS	GRXN0	147	PEX_RX0#	279
PEG_RXP1	SCD1U10V2KX-5GP	C440	DIS	GRXP1	143	PEX_RX1	278
PEG_RXN1	SCD1U10V2KX-5GP	C439	DIS	GRXN1	141	PEX_RX1#	280
PEG_RXP2	SCD1U10V2KX-5GP	C438	DIS	GRXP2	137	PEX_RX2	281
PEG_RXN2	SCD1U10V2KX-5GP	C437	DIS	GRXN2	135	PEX_RX2#	282
PEG_RXP3	SCD1U10V2KX-5GP	C436	DIS	GRXP3	123	PEX_RX3	283
PEG_RXN3	SCD1U10V2KX-5GP	C435	DIS	GRXN3	121	PEX_RX3#	284
PEG_RXP4	SCD1U10V2KX-5GP	C446	DIS	GRXP4	117	PEX_RX4	285
PEG_RXN4	SCD1U10V2KX-5GP	C445	DIS	GRXN4	115	PEX_RX4#	286
PEG_RXP5	SCD1U10V2KX-5GP	C434	DIS	GRXP5	111	PEX_RX5	287
PEG_RXN5	SCD1U10V2KX-5GP	C433	DIS	GRXN5	109	PEX_RX5#	288
PEG_RXP6	SCD1U10V2KX-5GP	C452	DIS	GRXP6	105	PEX_RX6	289
PEG_RXN6	SCD1U10V2KX-5GP	C451	DIS	GRXN6	103	PEX_RX6#	290
PEG_RXP7	SCD1U10V2KX-5GP	C432	DIS	GRXP7	97	PEX_RX7	291
PEG_RXN7	SCD1U10V2KX-5GP	C431	DIS	GRXN7	92	PEX_RX7#	292
PEG_RXP8	SCD1U10V2KX-5GP	C455	DIS	GRXP8	93	PEX_RX8	293
PEG_RXN8	SCD1U10V2KX-5GP	C454	DIS	GRXN8	91	PEX_RX8#	294
PEG_RXP9	SCD1U10V2KX-5GP	C430	DIS	GRXP9	87	PEX_RX9	295
PEG_RXN9	SCD1U10V2KX-5GP	C429	DIS	GRXN9	85	PEX_RX9#	296
PEG_RXP10	SCD1U10V2KX-5GP	C428	DIS	GRXP10	81	PEX_RX10	297
PEG_RXN10	SCD1U10V2KX-5GP	C427	DIS	GRXN10	79	PEX_RX10#	298
PEG_RXP11	SCD1U10V2KX-5GP	C450	DIS	GRXP11	75	PEX_RX11	299
PEG_RXN11	SCD1U10V2KX-5GP	C449	DIS	GRXN11	73	PEX_RX11#	300
PEG_RXP12	SCD1U10V2KX-5GP	C426	DIS	GRXP12	69	PEX_RX12	301
PEG_RXN12	SCD1U10V2KX-5GP	C425	DIS	GRXN12	67	PEX_RX12#	302
PEG_RXP13	SCD1U10V2KX-5GP	C424	DIS	GRXP13	63	PEX_RX13	303
PEG_RXN13	SCD1U10V2KX-5GP	C423	DIS	GRXN13	61	PEX_RX13#	304
PEG_RXP14	SCD1U10V2KX-5GP	C448	DIS	GRXP14	57	PEX_RX14	305
PEG_RXN14	SCD1U10V2KX-5GP	C447	DIS	GRXN14	55	PEX_RX14#	306
PEG_RXP15	SCD1U10V2KX-5GP	C422	DIS	GRXP15	51	PEX_RX15	307
PEG_RXN15	SCD1U10V2KX-5GP	C421	DIS	GRXN15	49	PEX_RX15#	308



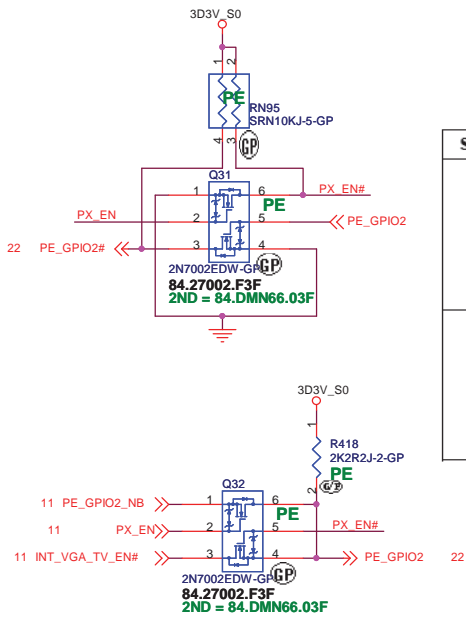
DP_A_AUX#	277	<< >>	NV_DVI_DAT_23
DP_A_AUX	279	<< >>	NV_DVI_CLK_23
DP_A_HPD	278	<< >>	MXM_DVI_HPD_23
DP_A_L0#	253	<< >>	TMDS_A_TX2_23
DP_A_L0	255	<< >>	TMDS_A_TX2+ 23
DP_A_L1#	259	<< >>	TMDS_A_TX1_23
DP_A_L1	261	<< >>	TMDS_A_TX1+ 23
DP_A_L2#	265	<< >>	TMDS_A_TX0_23
DP_A_L2	267	<< >>	TMDS_A_TX0+ 23
DP_A_L3#	271	<< >>	TMDS_A_TXC_23
DP_A_L3	273	<< >>	TMDS_A_TXC+ 23
DP_B_AUX#	270	<< >>	
DP_B_AUX	272	<< >>	
DP_B_HPD	274	<< >>	
DP_B_L0#	246	<< >>	
DP_B_L0	248	<< >>	
DP_B_L1#	252	<< >>	
DP_B_L1	254	<< >>	
DP_B_L2#	260	<< >>	
DP_B_L2	262	<< >>	
DP_B_L3#	266	<< >>	
DP_B_L3	268	<< >>	
DP_C_AUX#	223	<< >>	
DP_C_AUX	225	<< >>	
DP_C_HPD	234	<< >>	
DP_D_AUX#	230	<< >>	
DP_D_AUX	232	<< >>	
DP_D_HPD	236	<< >>	
DP_D_L0#	206	<< >>	
DP_D_L0	208	<< >>	
DP_D_L1#	212	<< >>	
DP_D_L1	214	<< >>	
DP_D_L2#	218	<< >>	
DP_D_L2	220	<< >>	
DP_D_L3#	224	<< >>	
DP_D_L3	226	<< >>	
VGA_DISABLE#	221	<< >>	
VGA_DDC_DATA	158	<< >>	CRT_DDCDATA_22
VGA_DDC_CLK	160	<< >>	CRT_DDCCLK_22
VGA_VSYNC	162	<< >>	CRT_VSYNC_22
VGA_HSYNC	164	<< >>	CRT_HSYNC_22
VGA_RED	168	<< >>	MXM_RED_20
VGA_GREEN	170	<< >>	MXM_GREEN_20
VGA_BLUE	172	<< >>	MXM_BLUE_20
GPIO0	26	<< >>	MXM_GPIO0_1
GPIO1	28	<< >>	MXM_GPIO1_1
GPIO2	30	<< >>	MXM_GPIO2_1



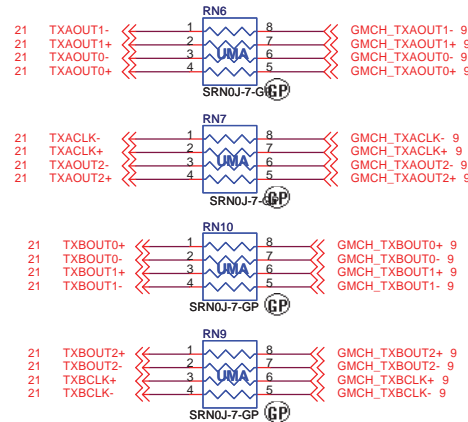
RSVD#159	159	<< >>	LVDS_UCLK#	169	<< >>	G72_TXBCLK_20
RSVD#161	161	<< >>	LVDS_UCLK	171	<< >>	G72_TXBCLK+ 20
RSVD#163	163	<< >>	LVDS_LCLK#	176	<< >>	G72_TXACLK_20
RSVD#165	165	<< >>	LVDS_LCLK	178	<< >>	G72_TXACLK+ 20
RSVD#167	167	<< >>	LVDS_DDC_CLK	35	<< >>	LCD_EDID_CLK_21
RSVD#227	227	<< >>	LVDS_DDC_DAT	33	<< >>	LCD_EDID_DAT_21
RSVD#231	231	<< >>	LVDS_UTX0	195	<< >>	G72_TXBOUT0+ 20
RSVD#233	233	<< >>	LVDS_UTX0#	193	<< >>	G72_TXBOUT0- 20
RSVD#235	235	<< >>	LVDS_UTX1	189	<< >>	G72_TXBOUT1+ 20
RSVD#237	237	<< >>	LVDS_UTX1#	187	<< >>	G72_TXBOUT1- 20
RSVD#239	239	<< >>	LVDS_UTX2	183	<< >>	G72_TXBOUT2+ 20
RSVD#241	241	<< >>	LVDS_UTX2#	181	<< >>	G72_TXBOUT2- 20
RSVD#243	243	<< >>	LVDS_UTX3	177	<< >>	
RSVD#245	245	<< >>	LVDS_UTX3#	175	<< >>	
RSVD#247	247	<< >>	LVDS_LTX0	202	<< >>	G72_TXAOUT0+ 20
RSVD#249	249	<< >>	LVDS_LTX0#	200	<< >>	G72_TXAOUT0- 20
RSVD#251	251	<< >>	LVDS_LTX1	196	<< >>	G72_TXAOUT1+ 20
RSVD#253	253	<< >>	LVDS_LTX1#	194	<< >>	G72_TXAOUT1- 20
RSVD#255	255	<< >>	LVDS_LTX2	190	<< >>	G72_TXAOUT2+ 20
RSVD#257	257	<< >>	LVDS_LTX2#	188	<< >>	G72_TXAOUT2- 20
RSVD#259	259	<< >>	LVDS_LTX3	184	<< >>	
RSVD#261	261	<< >>	LVDS_LTX3#	182	<< >>	
PWR_GOOD	6	<< >>	PRSNL_L#	281	<< >>	MXM_P_L_1
PWR_EN	18	<< >>	PRSNL_R#	282	<< >>	MXM_P_R_1
PWR_LEVEL	18	<< >>	PNL_BL_EN	25	<< >>	MXM_BLOIN
PWR_SRC#E1_1	E1.1	<< >>	PNL_PWR_EN	23	<< >>	MXM_PWN
PWR_SRC#E1_2	E1.2	<< >>	TH_OVERT#	20	<< >>	MXM_THER
PWR_SRC#E1_3	E1.3	<< >>	TH_ALERT#	22	<< >>	MXM_THA
PWR_SRC#E1_4	E1.4	<< >>	WAKE#	4	<< >>	MXM_WAKE_1
PWR_SRC#E1_5	E1.5	<< >>	HDMI_CEC	29	<< >>	MXM_HD_CEC_1
PWR_SRC#E1_6	E1.6	<< >>	CLK_REQ#	154	<< >>	MXM_CLK_R_1
PWR_SRC#E1_7	E1.7	<< >>	TH_PWM	24	<< >>	MXM_TH_PWM
PWR_SRC#E1_8	E1.8	<< >>	DVI_HPD	31	<< >>	MXM_DVI_HPD
PWR_SRC#E1_9	E1.9	<< >>	OEM#38	38	<< >>	
PWR_SRC#E2_1	E2.1	<< >>	OEM#39	39	<< >>	
PWR_SRC#E2_2	E2.2	<< >>	OEM#40	40	<< >>	
PWR_SRC#E2_3	E2.3	<< >>	OEM#41	41	<< >>	
PWR_SRC#E2_4	E2.4	<< >>	OEM#42	42	<< >>	
PWR_SRC#E2_5	E2.5	<< >>	OEM#43	43	<< >>	
PWR_SRC#E2_6	E2.6	<< >>	OEM#44	44	<< >>	
PWR_SRC#E2_7	E2.7	<< >>	OEM#45	45	<< >>	
PWR_SRC#E2_8	E2.8	<< >>				
PWR_SRC#E2_9	E2.9	<< >>				



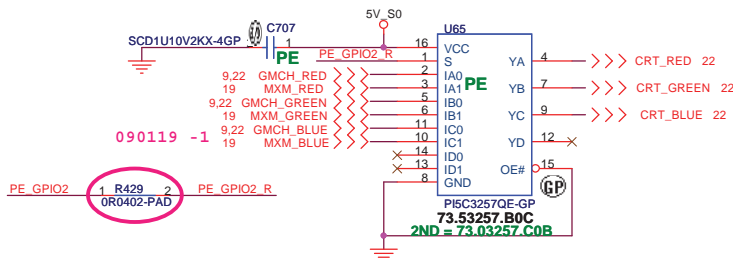
1	5V	GND	179
3	5V	GND	185
5	5V	GND	191
7	5V	GND	197
9	5V	GND	203
11	5V	GND	209
13	5V	GND	215
15	5V	GND	221
17	5V	GND	227
19	5V	GND	233
21	5V	GND	239
23	5V	GND	245
25	5V	GND	251
27	5V	GND	257
29	5V	GND	263
31	5V	GND	269
33	5V	GND	275
35	5V	GND	281
37	5V	GND	287
39	5V	GND	293
41	5V	GND	299
43	5V	GND	305
45	5V	GND	311
47	5V	GND	317
49	5V	GND	323
51	5V	GND	329
53	5V	GND	335
55	5V	GND	341
57	5V	GND	347
59	5V	GND	353
61	5V	GND	359
63	5V	GND	365
65	5V	GND	371
67	5V	GND	377
69	5V	GND	383
71	5V	GND	389
73	5V	GND	395
75	5V	GND	401
77	5V	GND	407
79	5V	GND	413
81	5V	GND	419
83	5V	GND	425
85	5V	GND	431
87	5V	GND	437
89	5V	GND	443
91	5V	GND	449
93	5V	GND	455
95	5V	GND	461
97	5V	GND	467
99	5V	GND	473
101	5V	GND	479
103	5V	GND	485
105	5V	GND	491
107	5V	GND	497
109	5V	GND	503
111	5V	GND	509
113	5V	GND	515
115	5V	GND	521
117	5V	GND	527
119	5V	GND	533
121	5V	GND	539
123	5V	GND	545
125	5V	GND	551
127	5V	GND	557
129	5V	GND	563
131	5V	GND	569
133	5V	GND	575
135	5V	GND	581
137	5V	GND	587
139	5V	GND	593
141	5V	GND	599
143	5V	GND	605
145	5V	GND	611
147	5V	GND	617
149	5V	GND	623
151	5V	GND	629
153	5V	GND	635
155	5V	GND	641
157	5V	GND	647
159	5V	GND	653
161	5V	GND	659
163	5V	GND	665
165	5V	GND	671
167	5V	GND	677
169	5V	GND	683
171	5V	GND	689
173	5V	GND	695
175	5V	GND	701
177	5V	GND	707
179	5V	GND	713
181	5V	GND	719
183	5V	GND	725
185	5V	GND	731
187	5V	GND	737
189	5V	GND	743
191	5V	GND	749
193	5V	GND	755
195	5V	GND	761
197	5V	GND	767
199	5V	GND	773
201	5V	GND	779
203	5V	GND	785
205	5V	GND	791
207	5V	GND	797
209	5V	GND	803
211	5V	GND	809
213	5V	GND	815</



FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



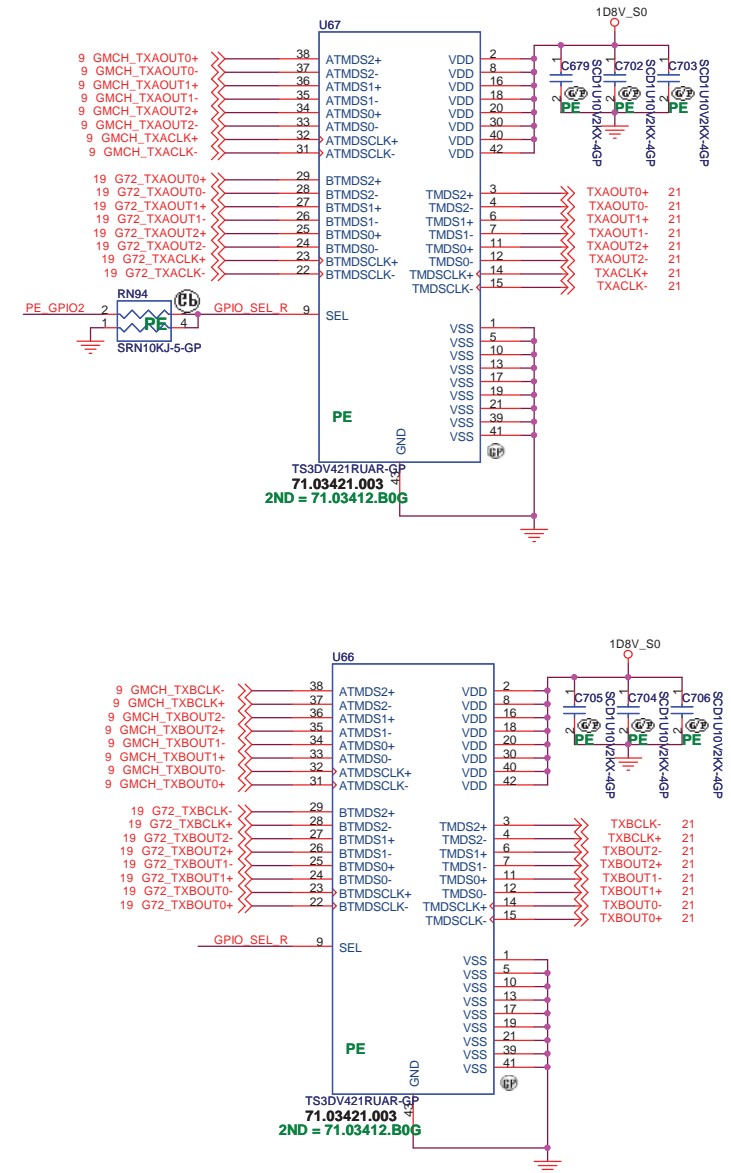
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DISPLAY SUPPORT TABLE

	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)

<http://hobi-elektronika.net>

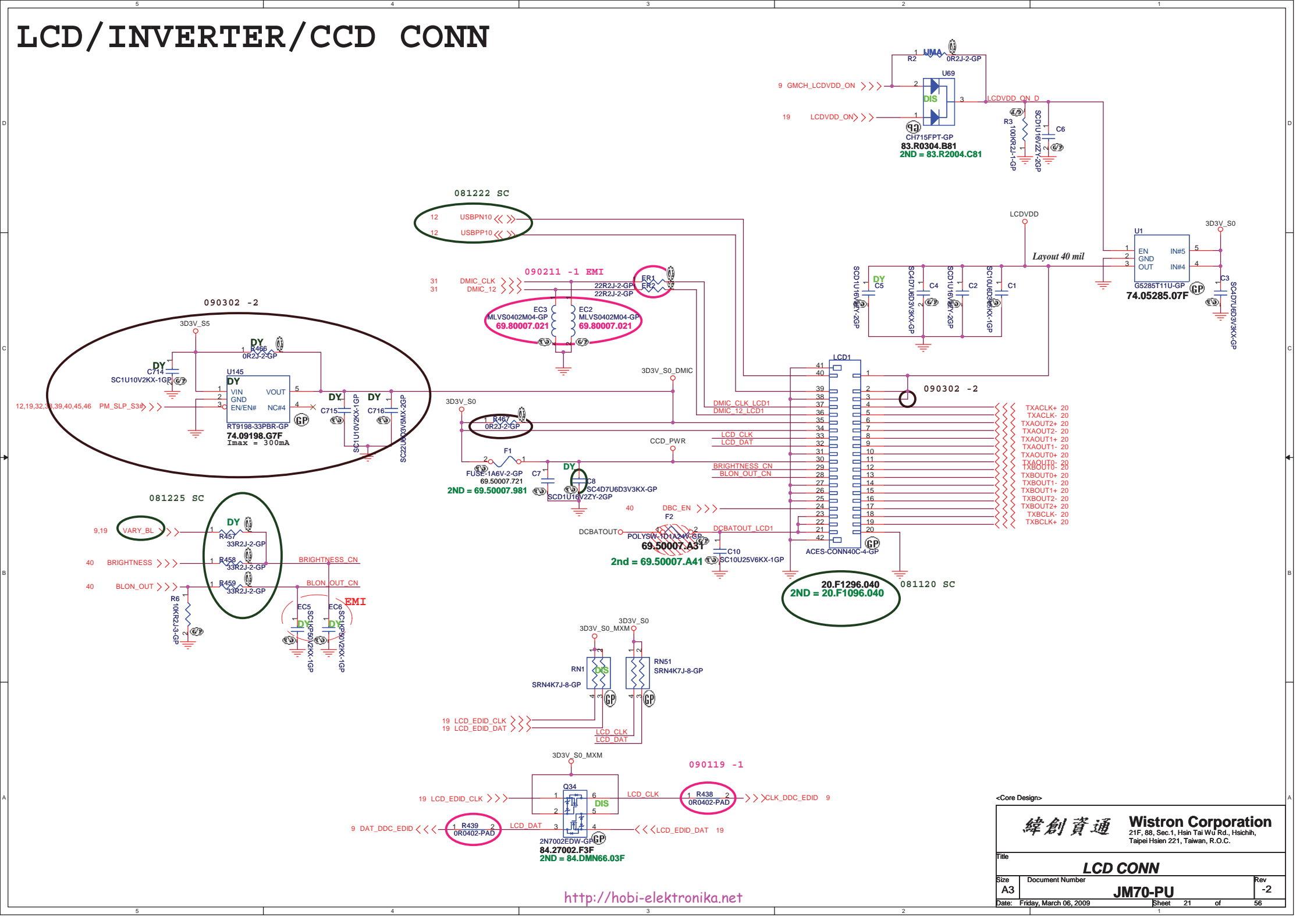
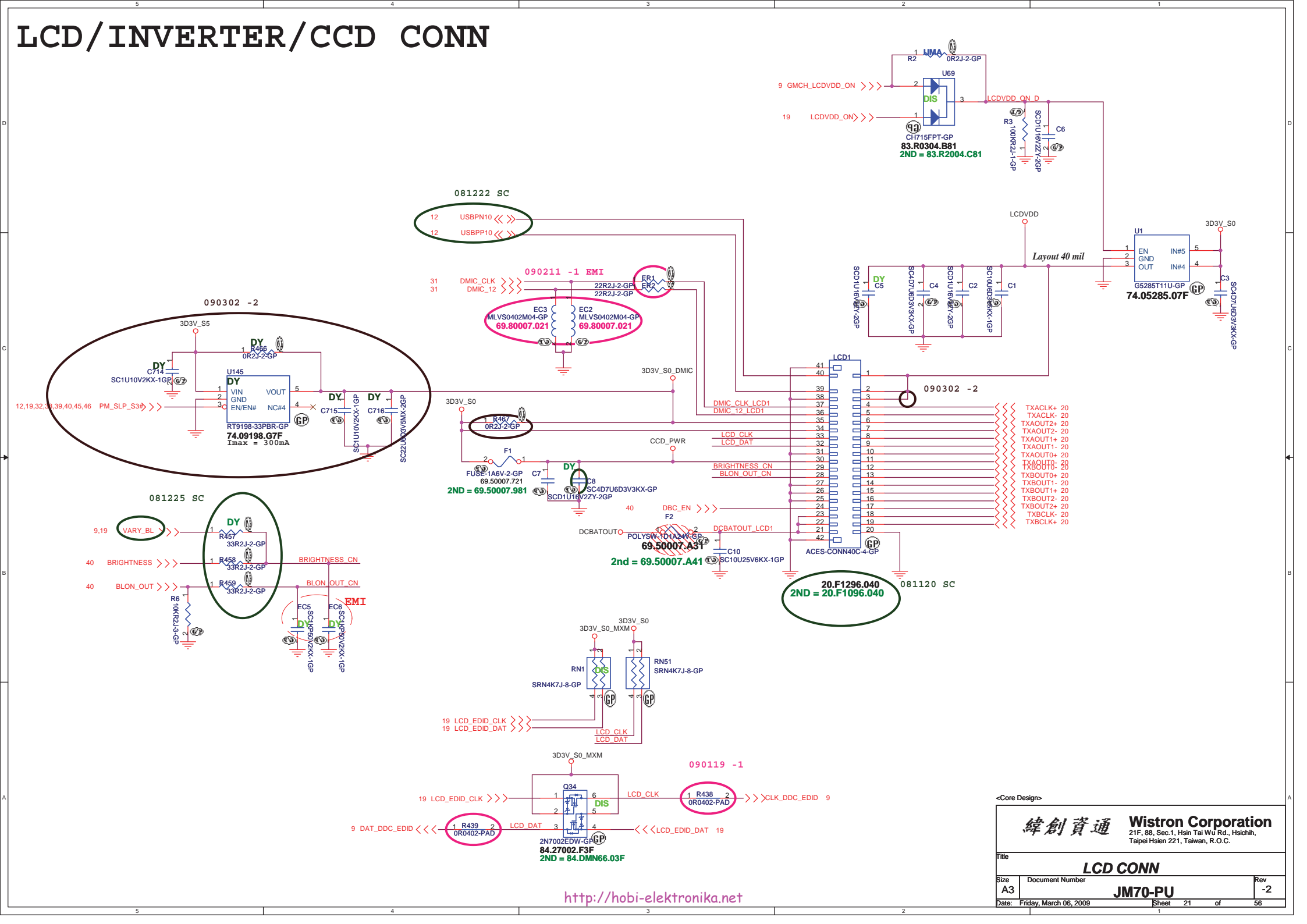
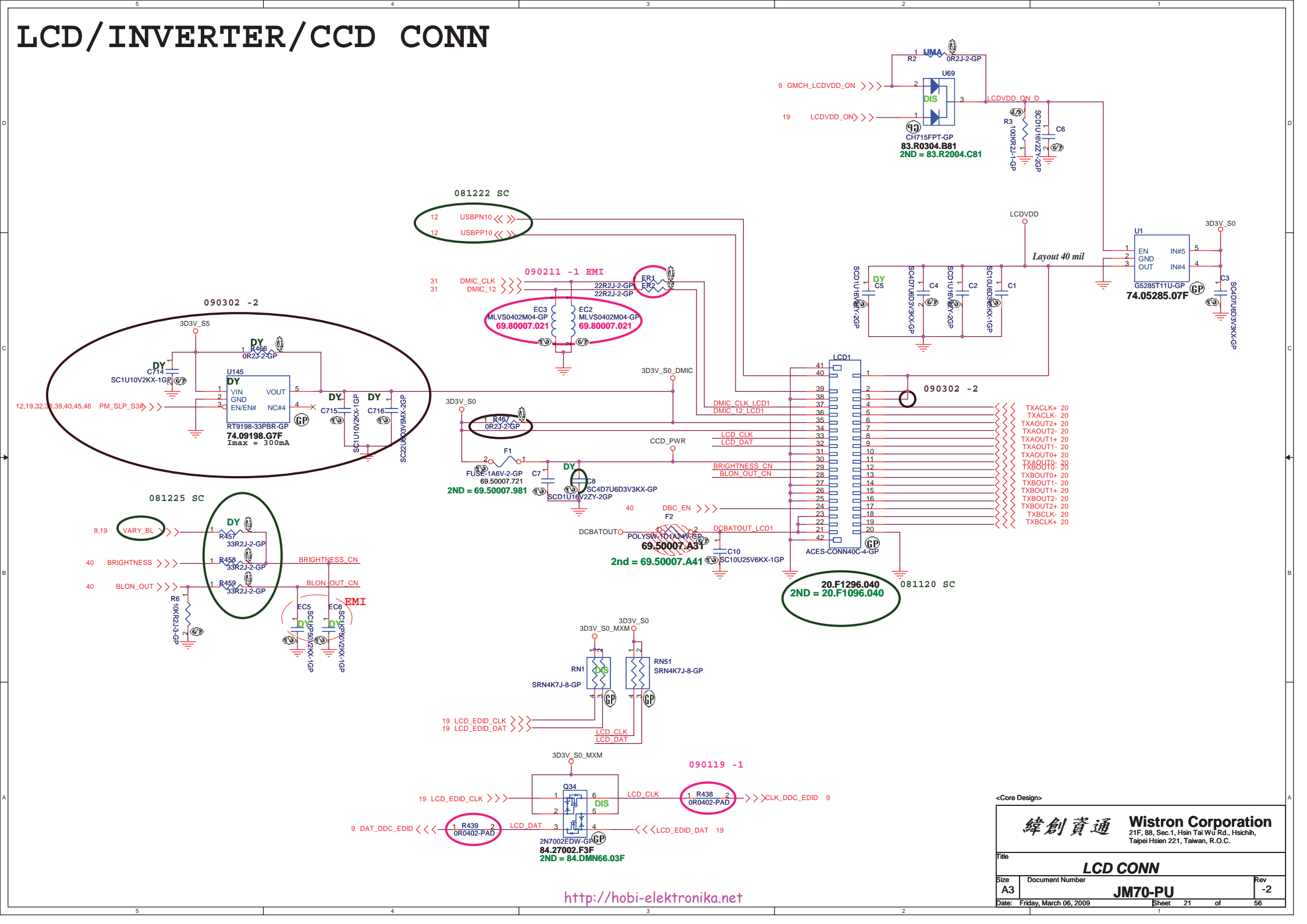
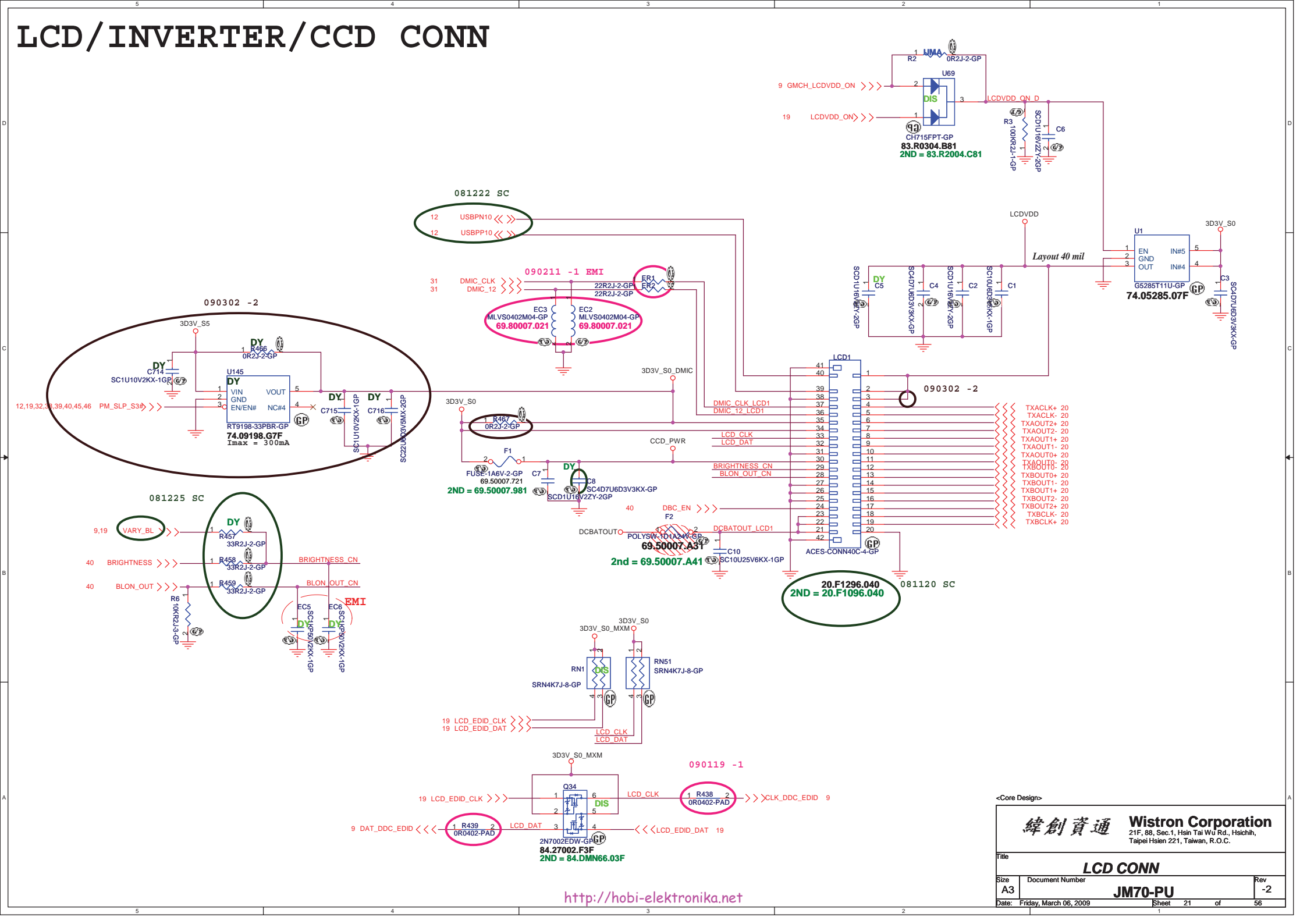
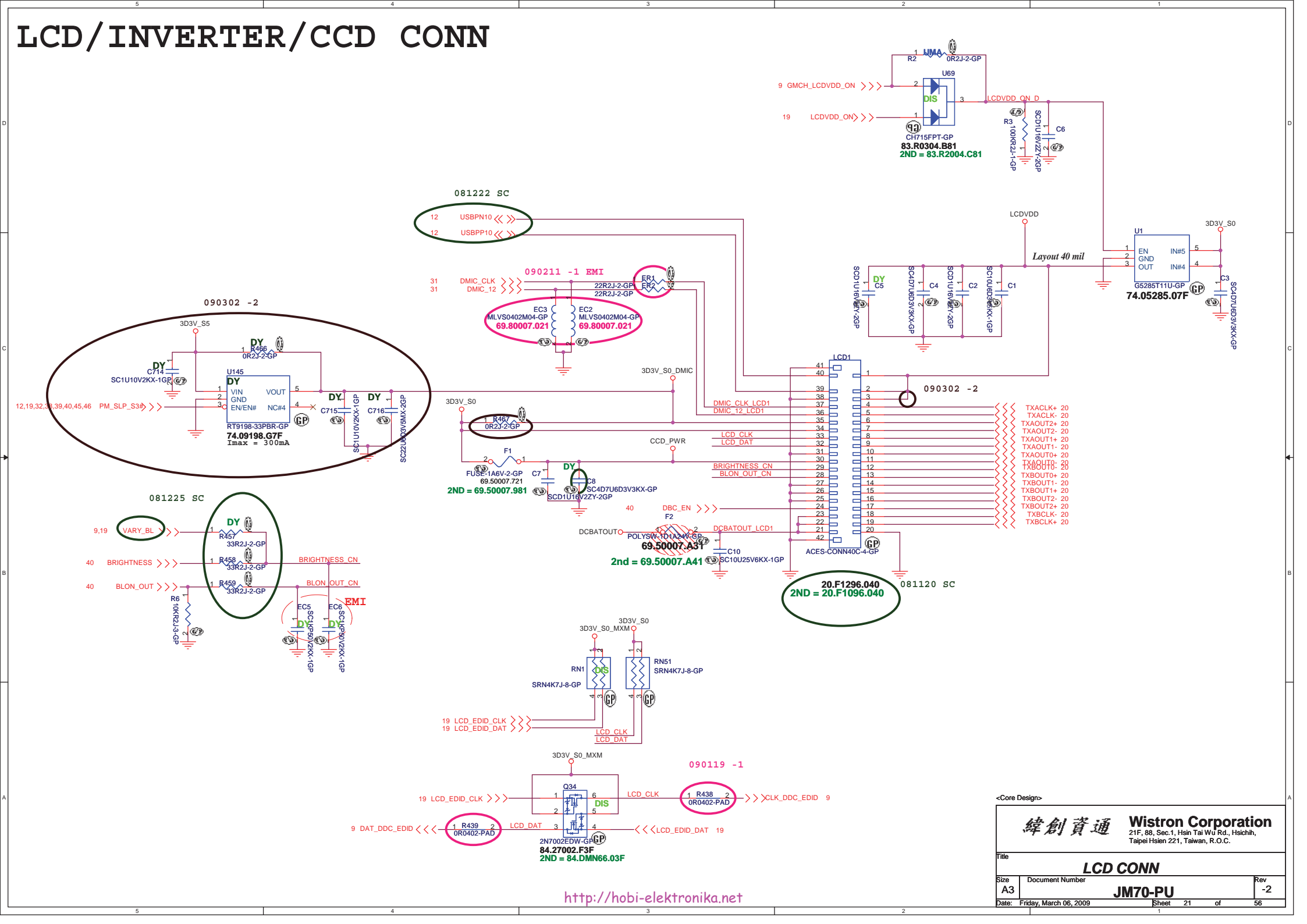


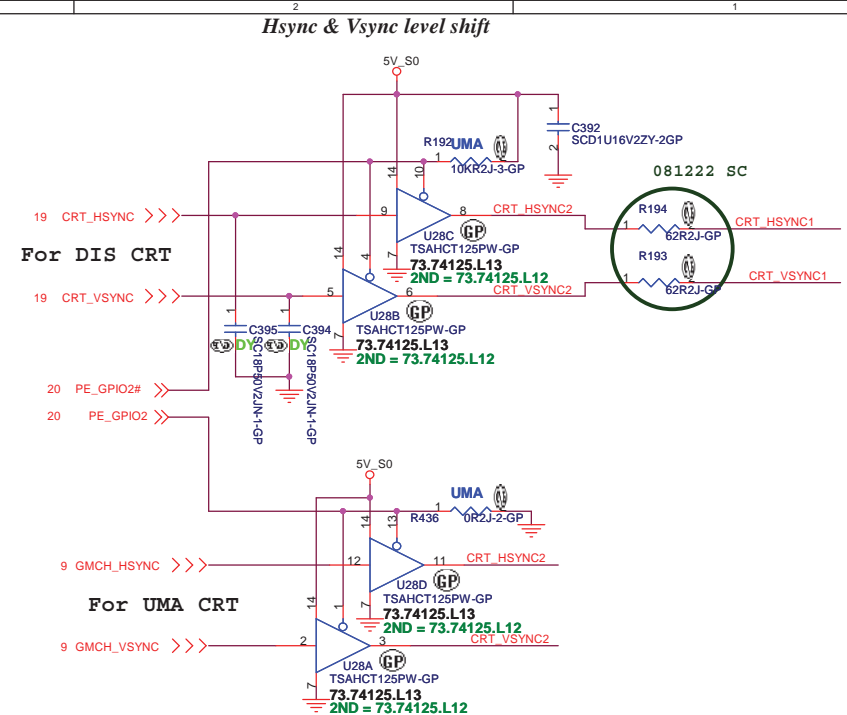
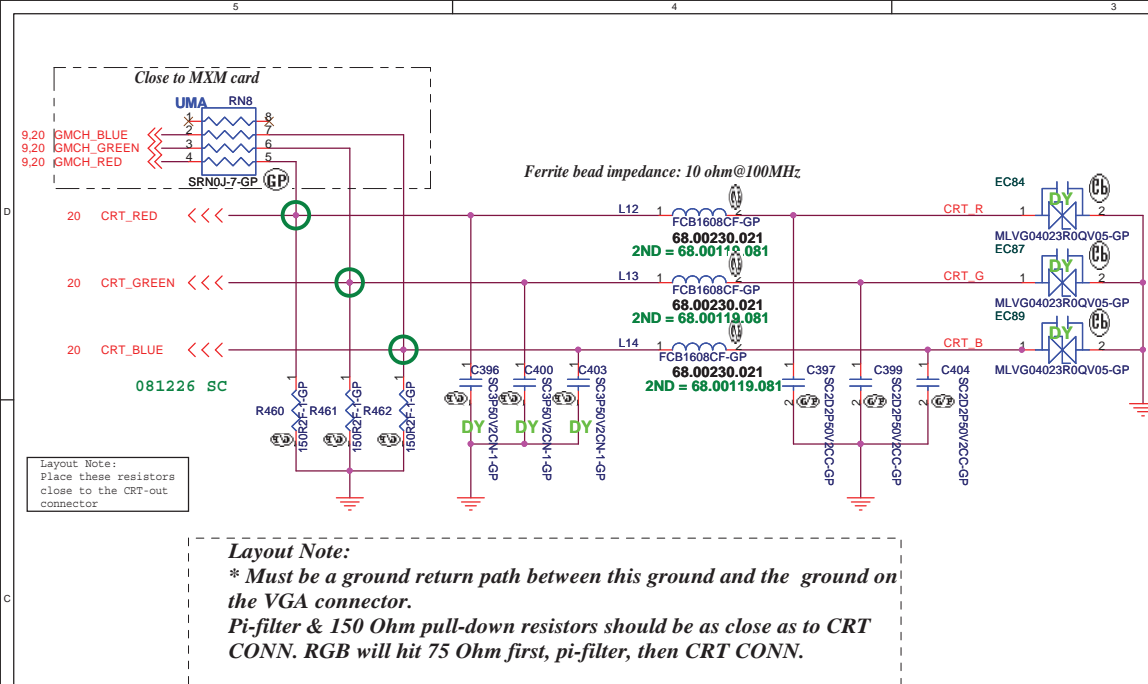
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

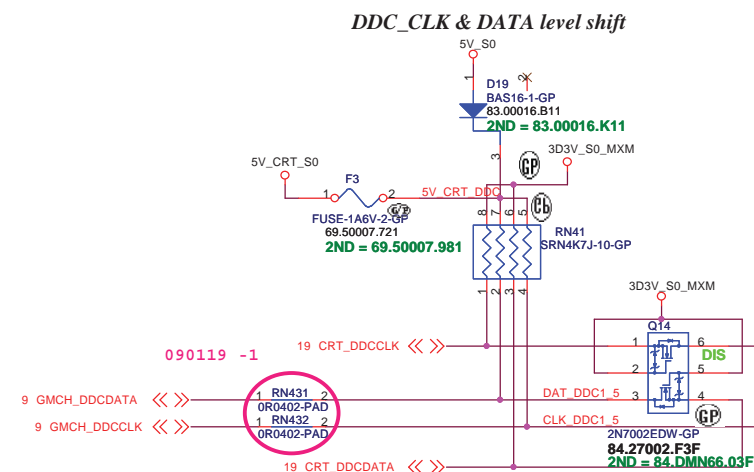
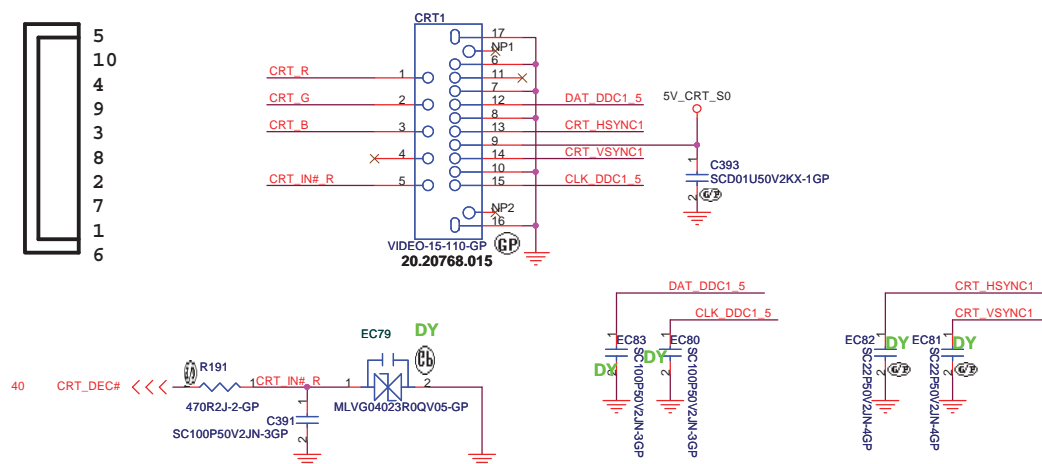
File: **SWITCH**
 Size: Document Number: **JM70-PU** Rev: -2

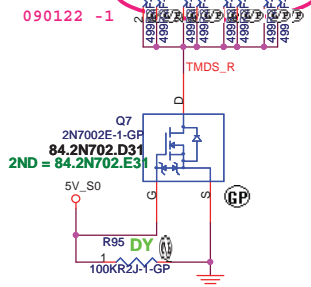
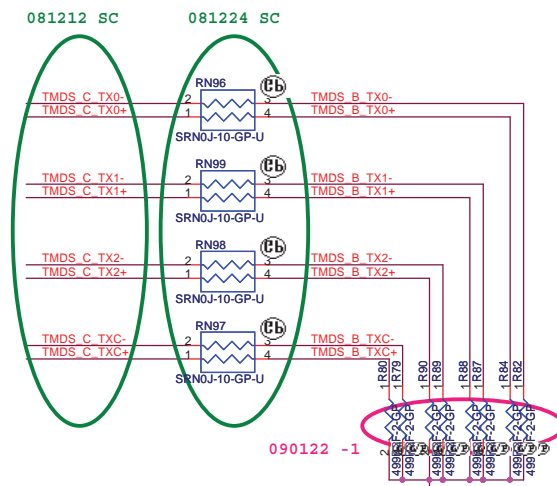
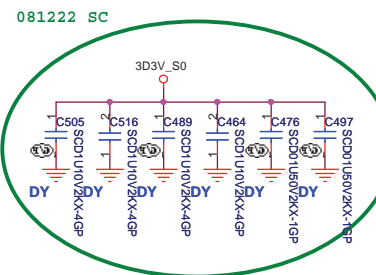
Date: Friday, March 06, 2009 Sheet 20 of 56

[illegible]

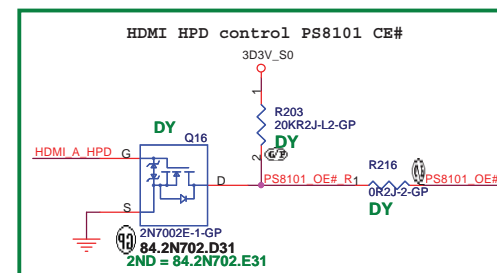
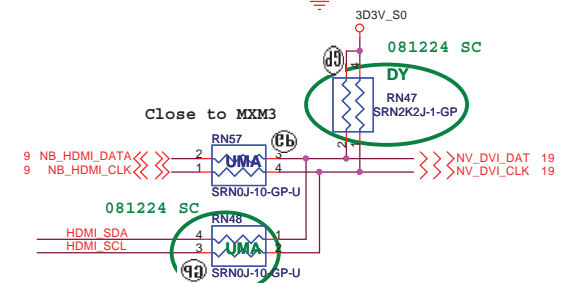
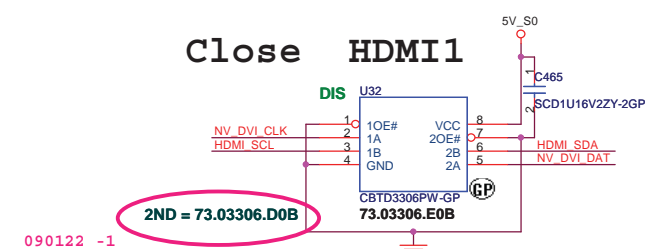


CRT I/F & CONNECTOR



[illegible]

Close HDMI1

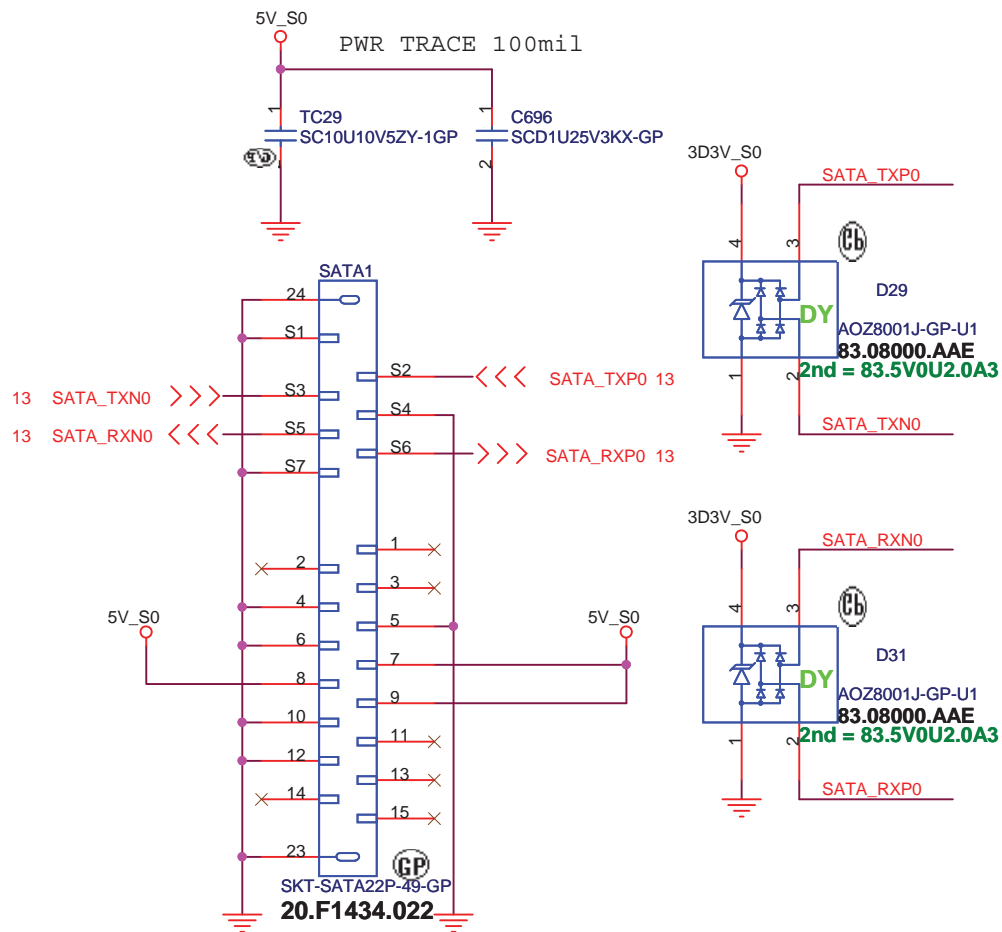


緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

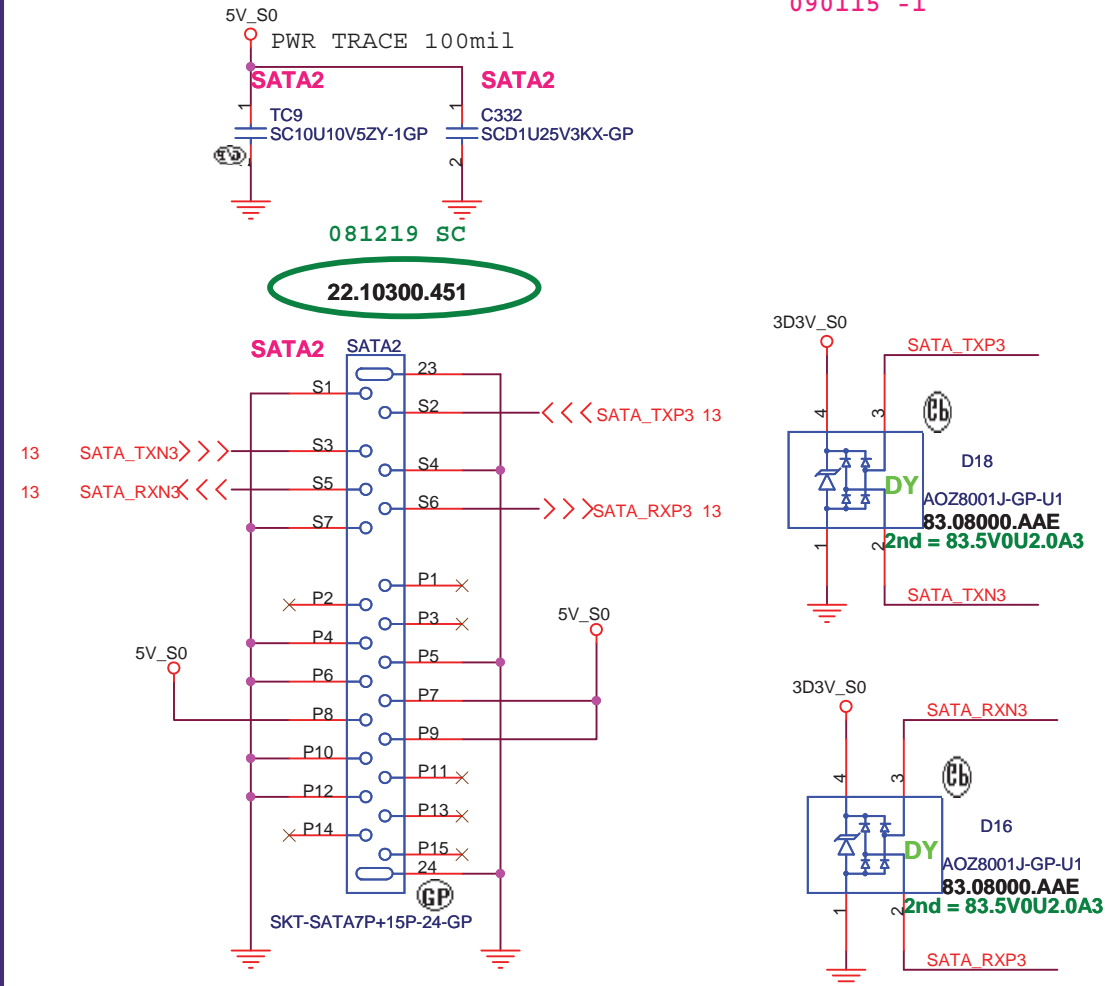
Title			
HDMI CONNECTOR			
Size	Document Number		Rev
A3	JM70-PU		.2
Date:	Friday, March 06, 2009	Sheet 23 of	56

SATA HDD Connector



2ND SATA HDD Connector

090115 -1



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD

Size

A4

Document Number

JM70-PU

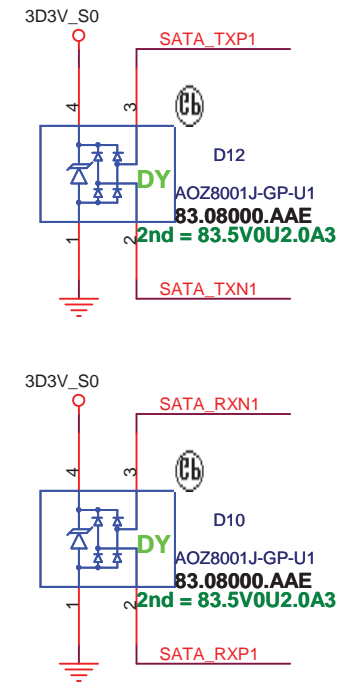
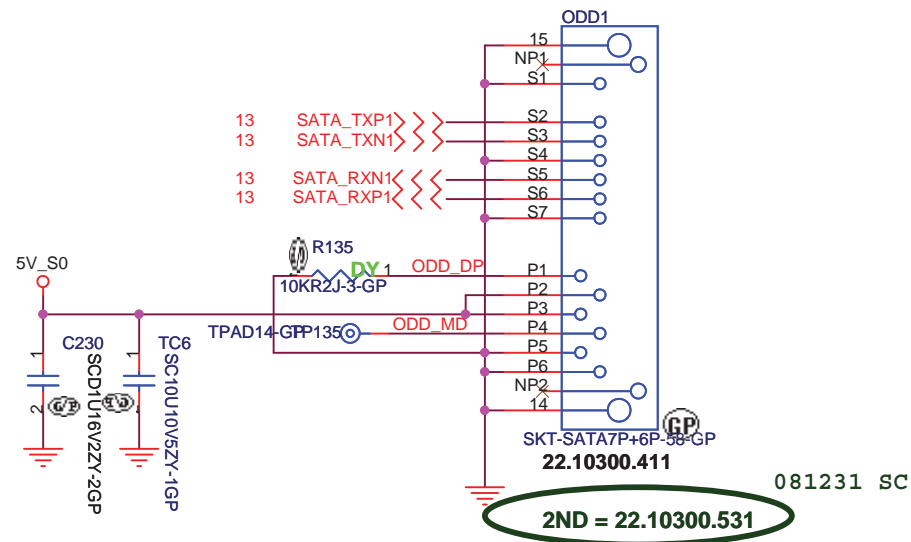
Rev

-2

Date: Friday, March 06, 2009

Sheet 24 of 56

ODD Connector



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CDROM

Size

Document Number

A4

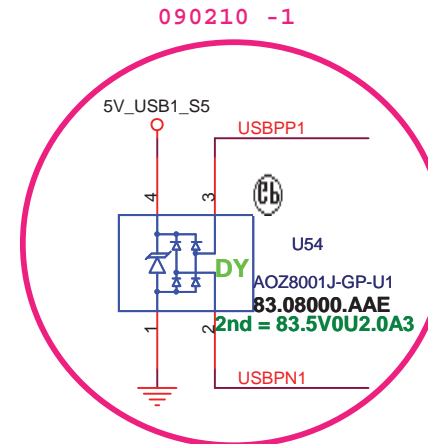
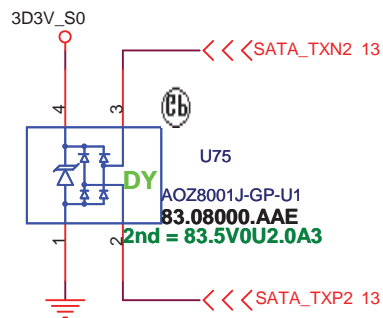
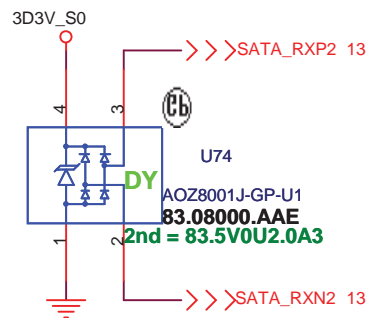
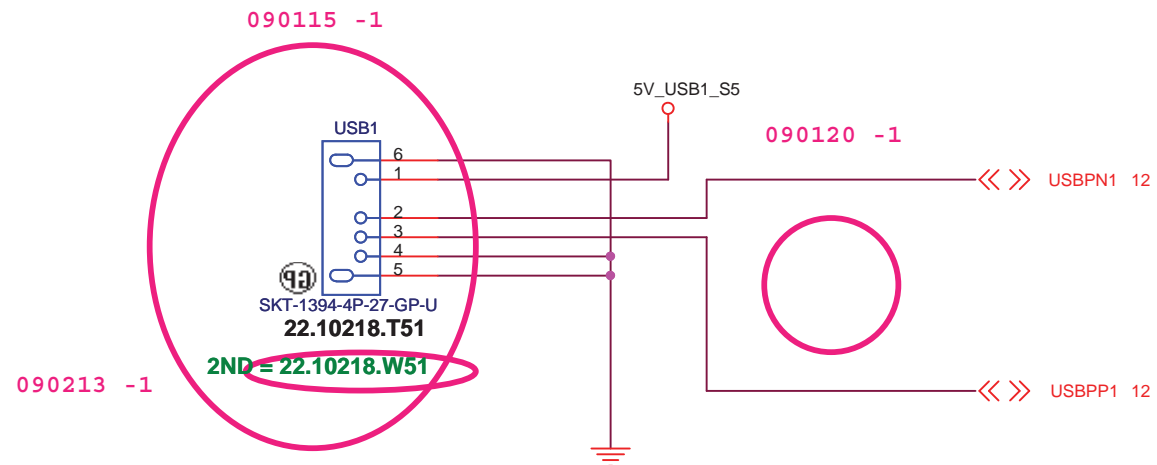
JM70-PU

Rev

-2

Date: Friday, March 06, 2009

Sheet 25 of 56

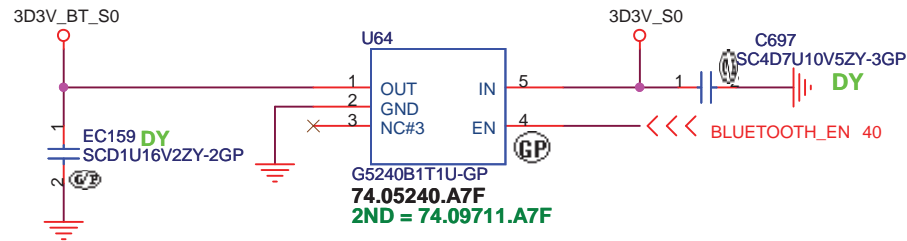


<Core Design>

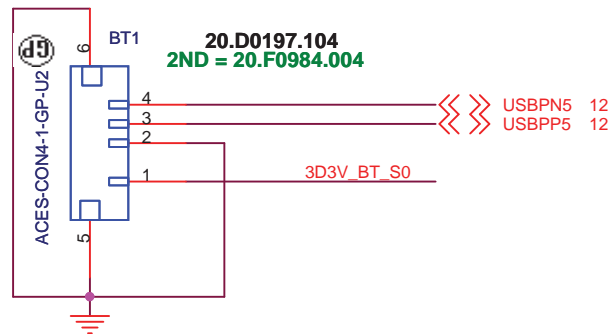
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			USB1
Size	Document Number	Rev	
A4	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	26 of 56

BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one
choke near connector by EMI request



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

A4

Document Number

JM70-PU

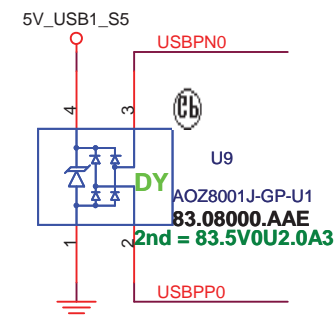
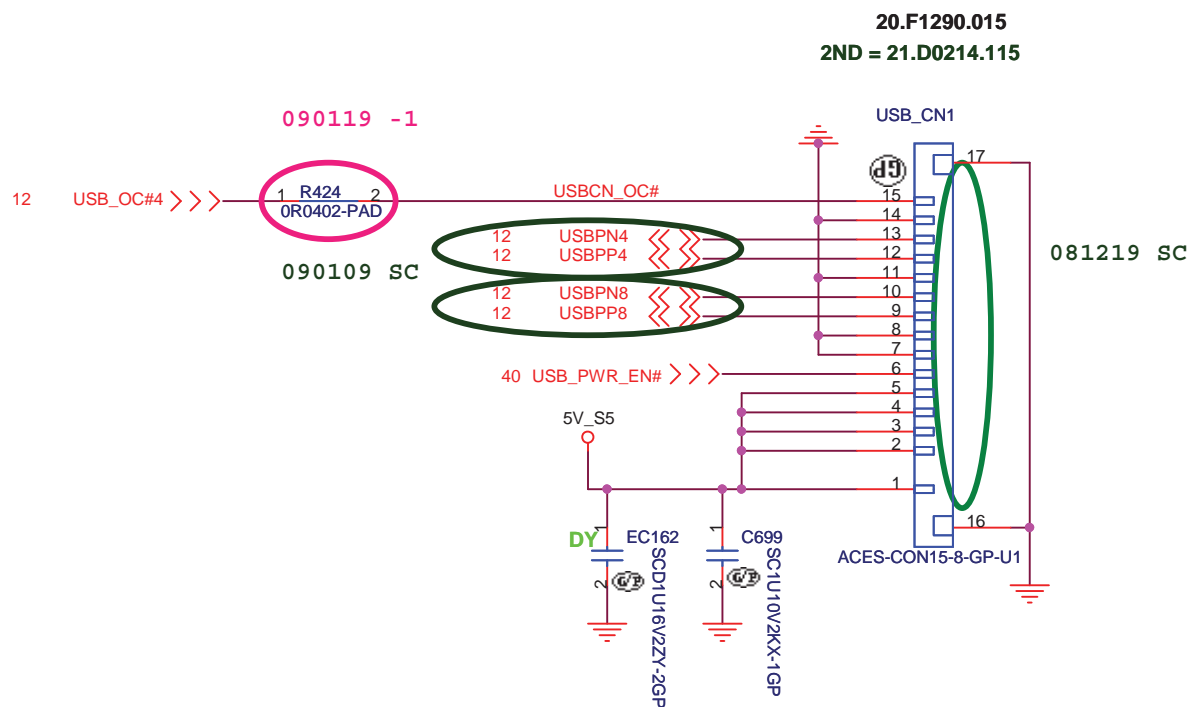
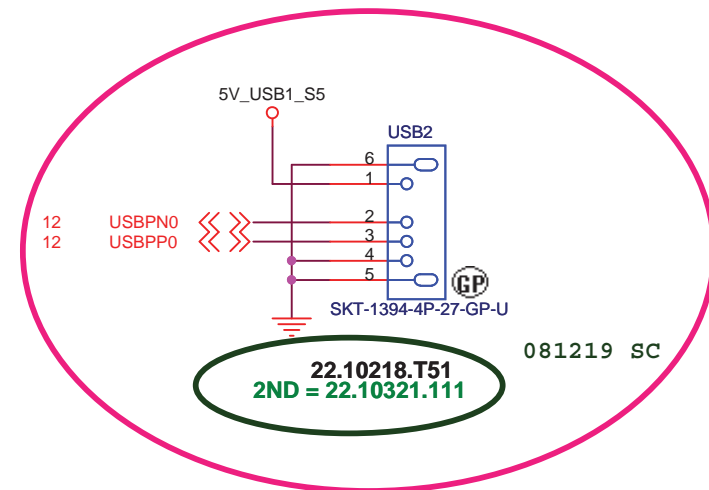
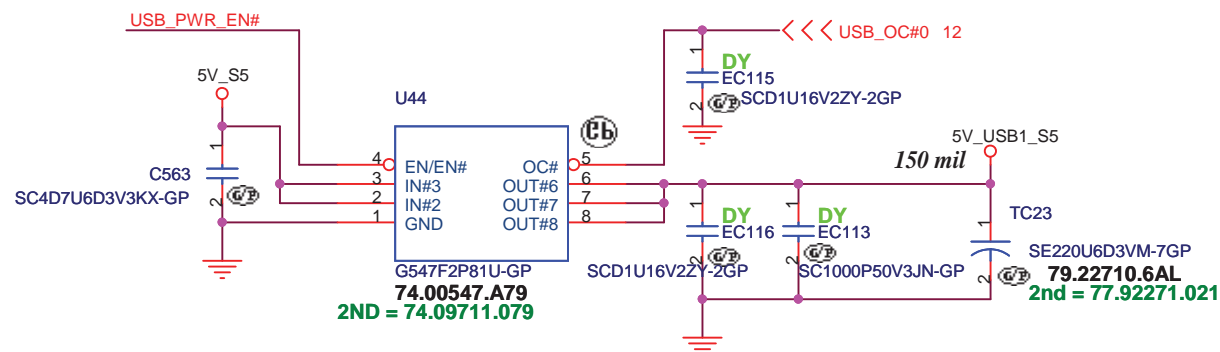
Rev

-2

Date: Friday, March 06, 2009

Sheet 27 of 56

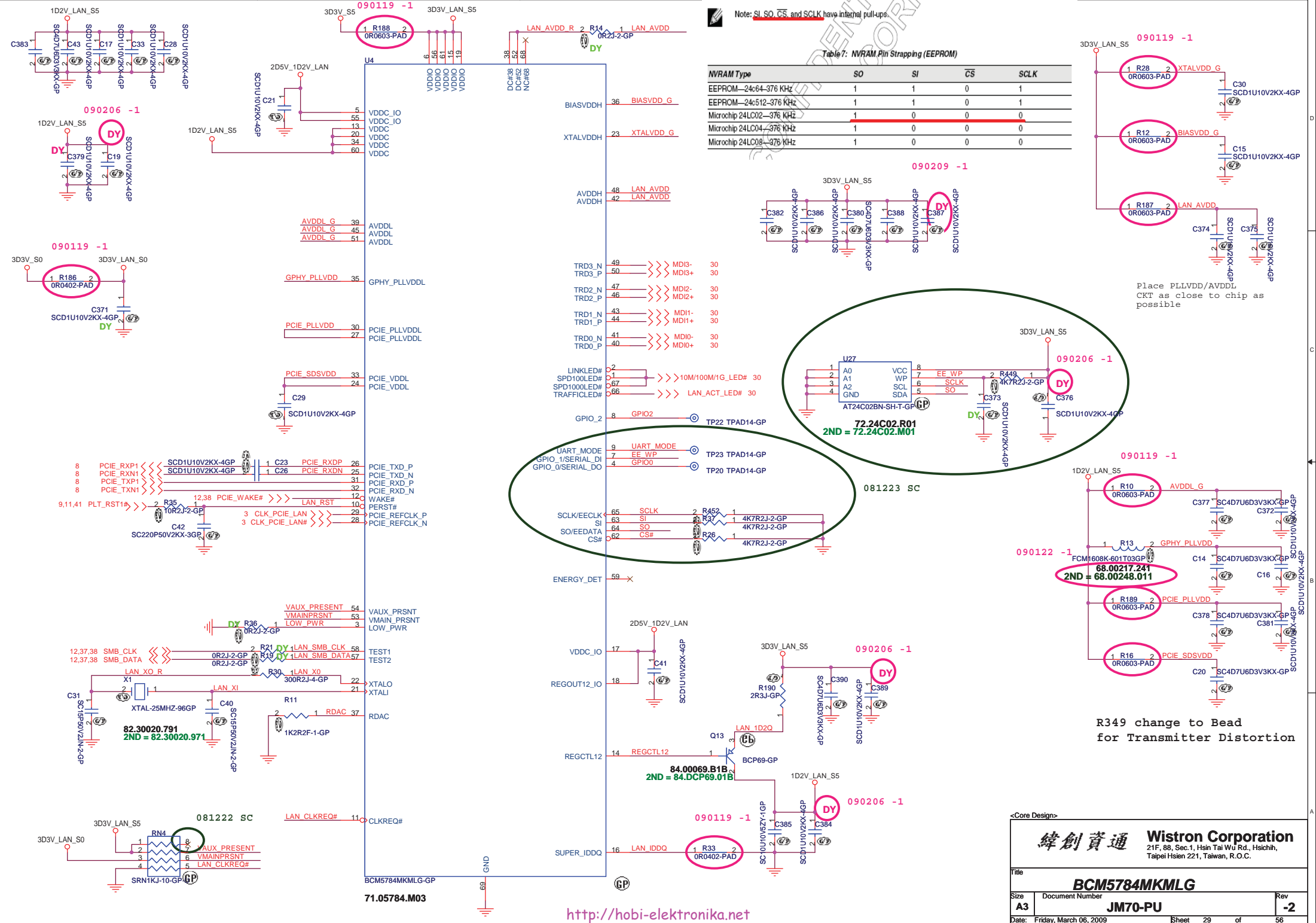
090115 -1



<Core Design>

<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p>USB2</p>	
<p>Size</p> <p>A4</p>	<p>Document Number</p> <p>JM70-PU</p>
<p>Date:</p> <p>Friday, March 06, 2009</p>	<p>Rev</p> <p>-2</p>
<p>Sheet 28 of 56</p>	

<http://hobi-elektronika.net>



Note: SI, SO, CS, and SCLK have internal pull-ups.

Table 7: NVRAM Pin Strapping (EEPROM)

NVRAM Type	SO	SI	CS	SCLK
EEPROM—24c64—376 KHz	1	1	0	1
EEPROM—24c512—376 KHz	1	1	0	1
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0

Place PLLVDD/AVDDL CKT as close to chip as possible

R349 change to Bead for Transmitter Distortion

<Core Design>

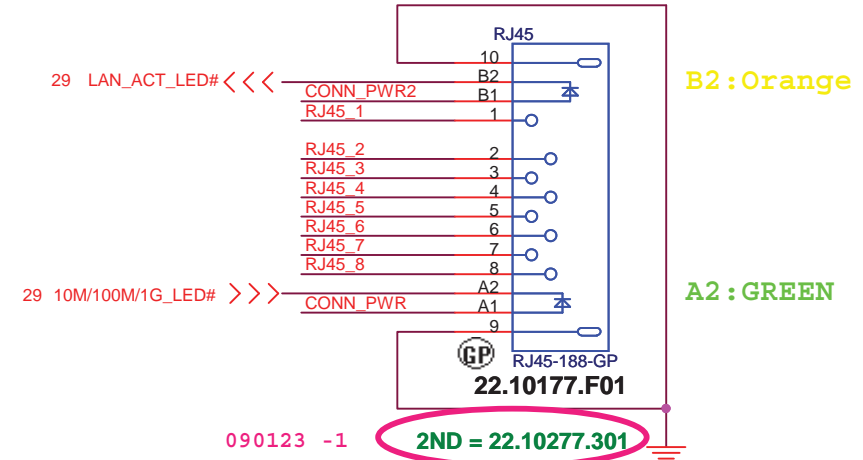
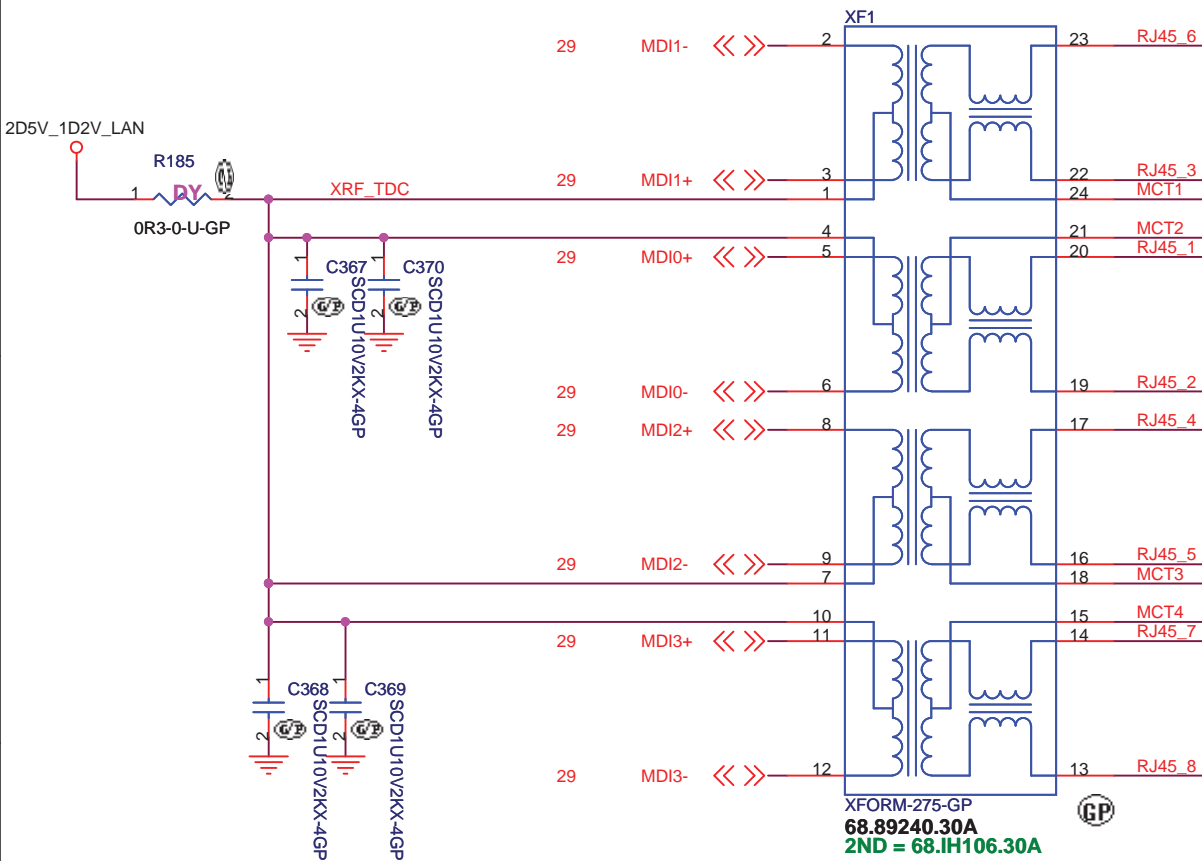
緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		BCM5784MKMLG	
Size	Document Number	Rev	
A3	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	29 of 56

LAN Connector



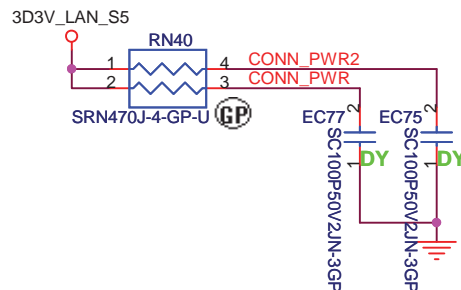
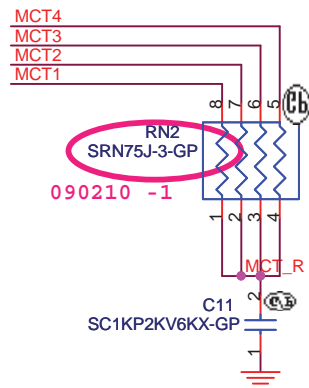
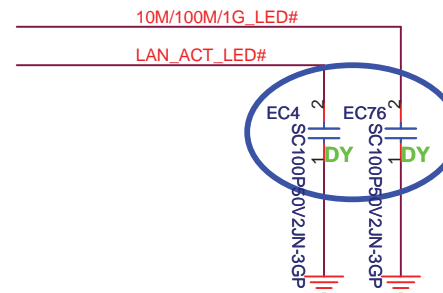
Green(A2), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<http://hobi-elektronika.net>

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN CONN

Size

A4

Document Number

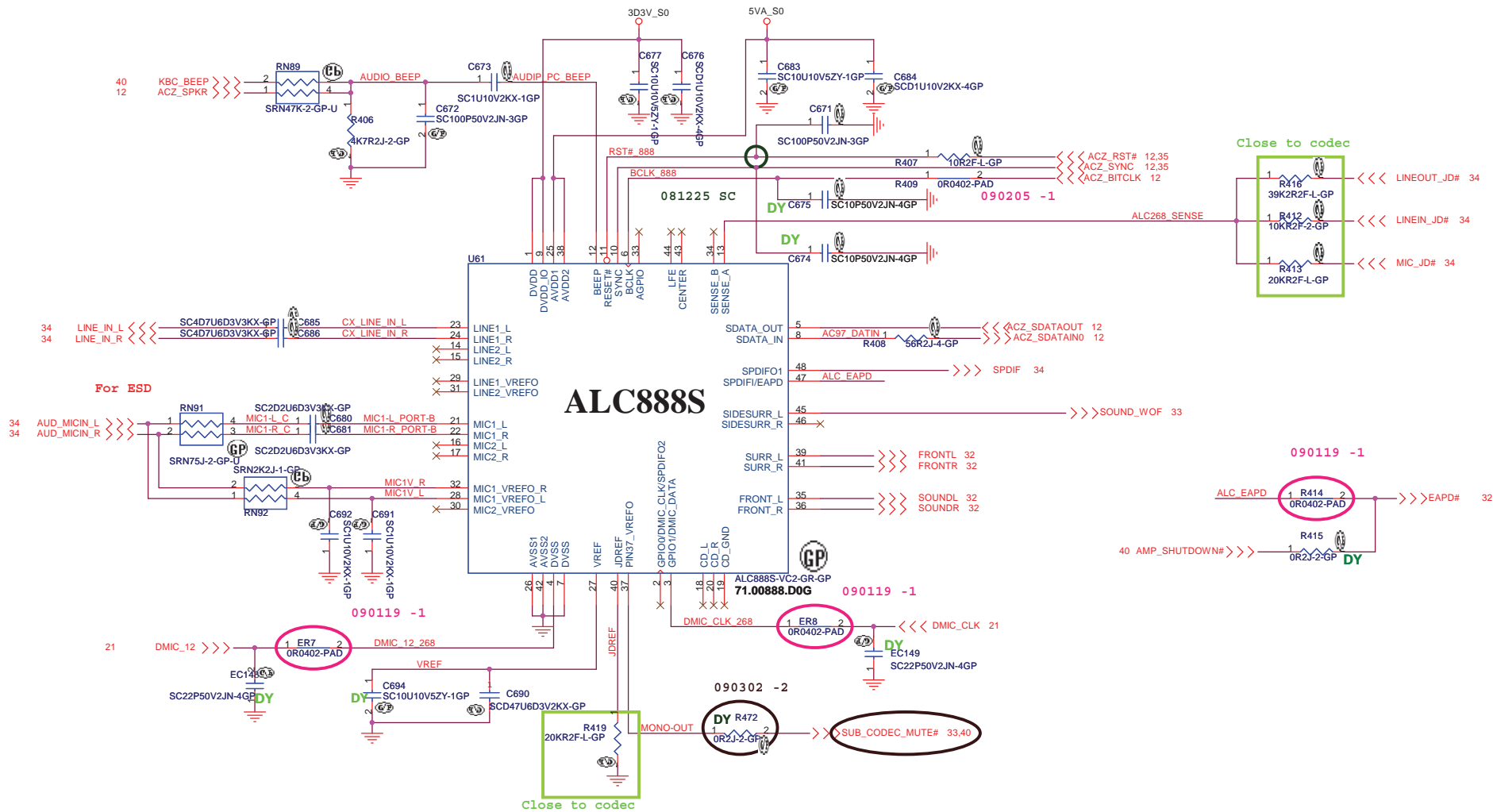
JM70-PU

Rev

-2

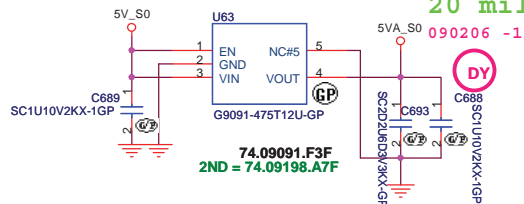
Date: Friday, March 06, 2009

Sheet 30 of 56



POWER GENERATE

Layout
20 mil



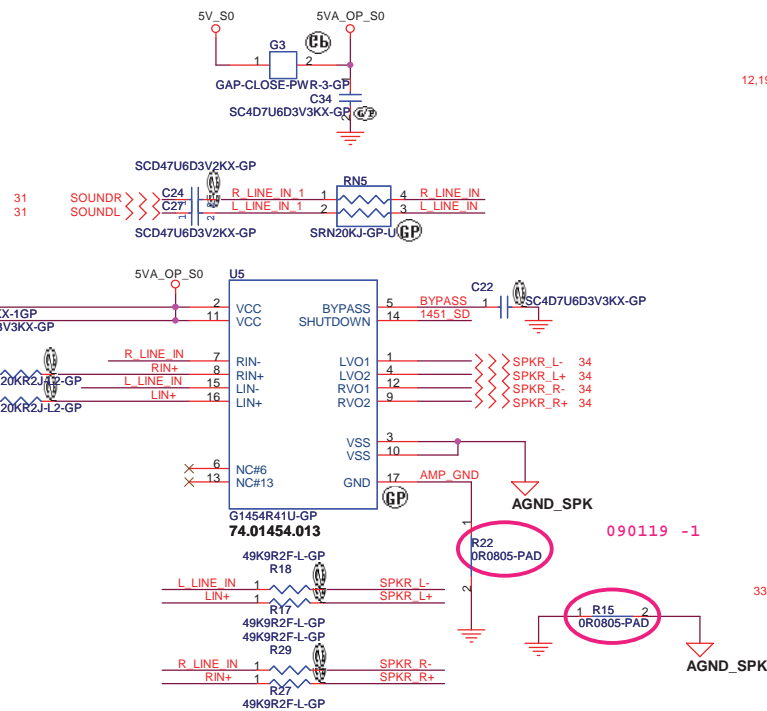
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

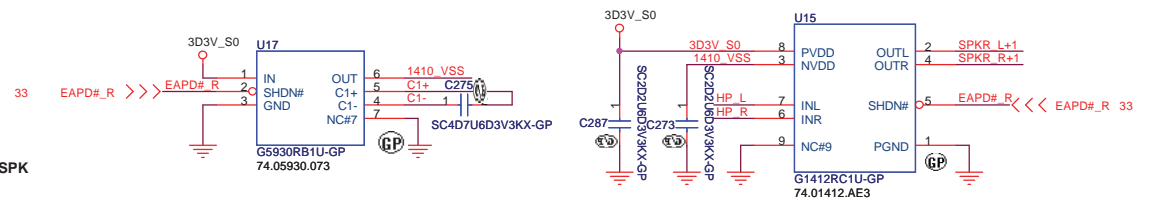
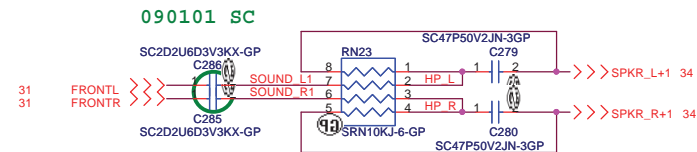
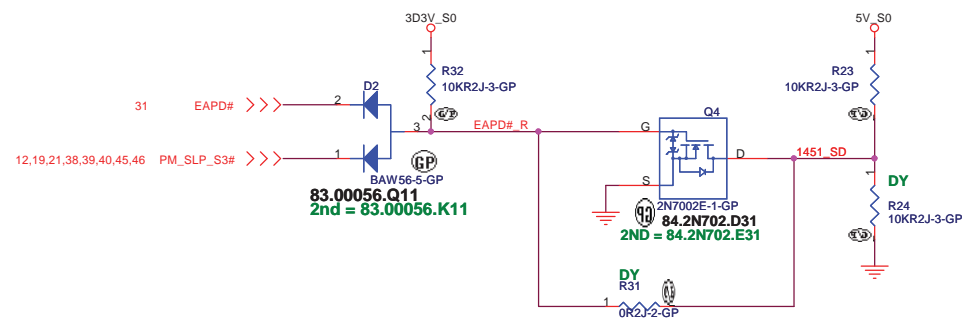
Title Azalia codec ALC268

Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 31 of 56	

AUDIO OP AMPLIFIER

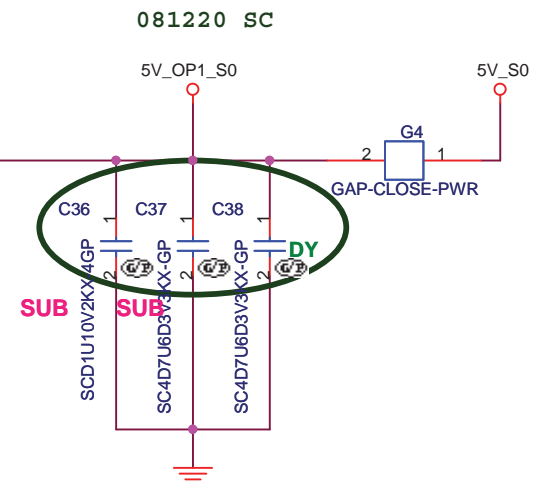
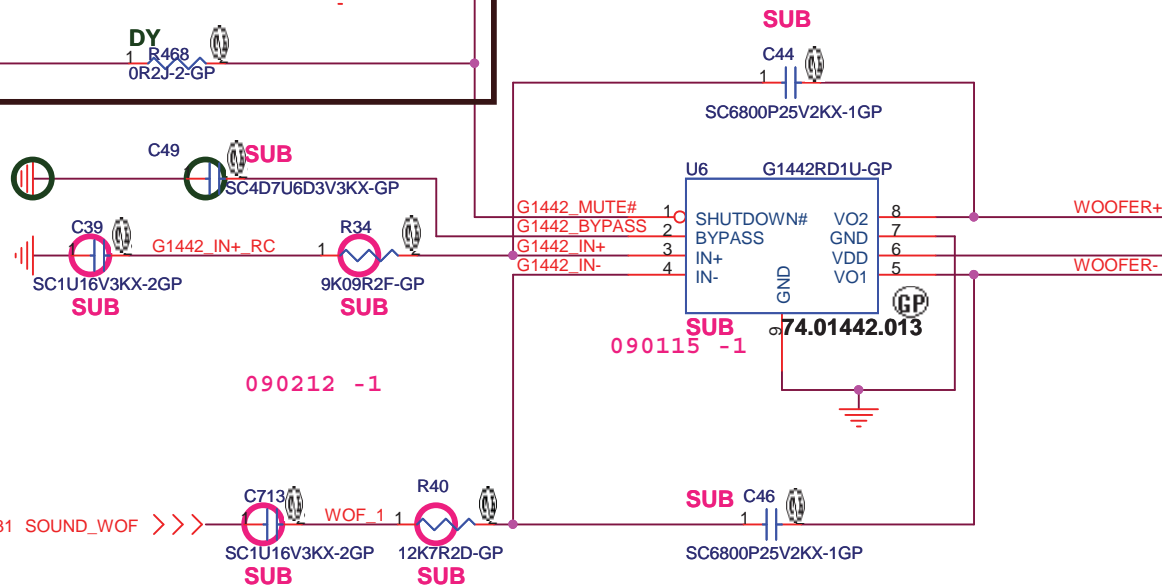
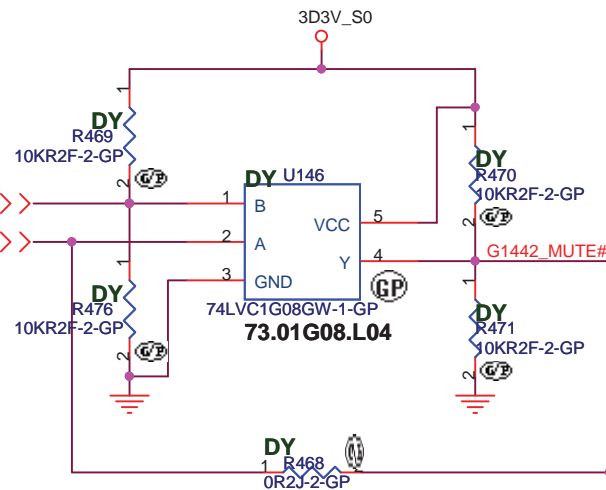


Gain= $R_f/R_i=49.9K/20K=2.495V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 $I_f \text{ VIN}=1.54V \text{ Gain}=2.6V/V \text{ RL}=4\Omega \text{ VO(peak)}=4V$
 $V(rms)=2.828V$
 $Power=2.828^2/4=1.999W$



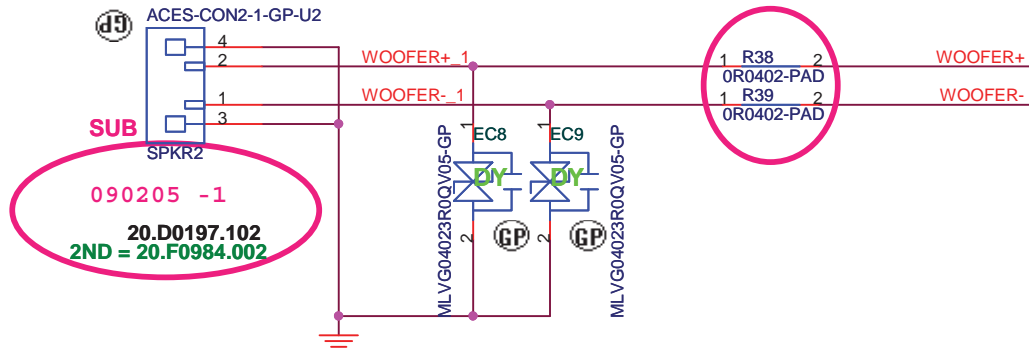
Gain= $R_f/R_i=20K/18K=0.9V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 $I_f \text{ VIN}=1.54V \text{ Gain}=0.9V/V \text{ RL}=4\Omega \text{ VO(peak)} = 4V \text{ V(rms)}=2.828V$
 Power= ?

090305 -2



SUBWOOFER CONN.

090119 -1



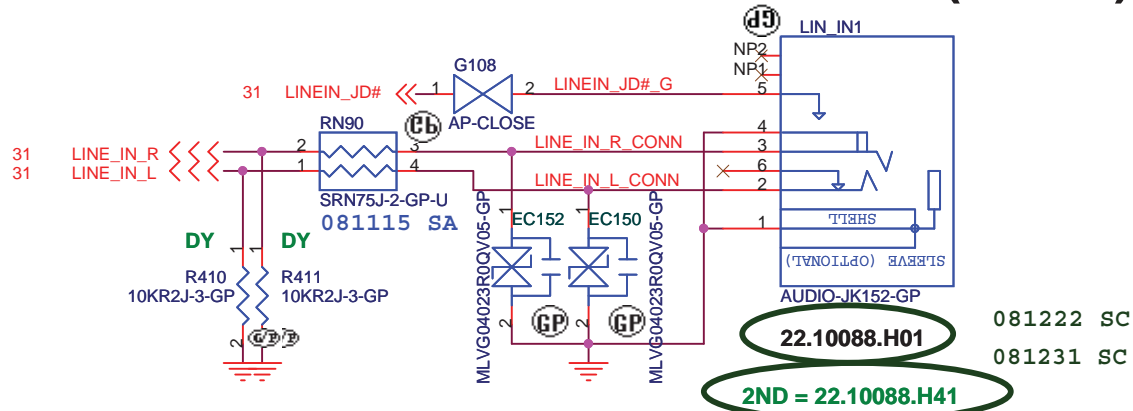
<Core Design>

緯創資通

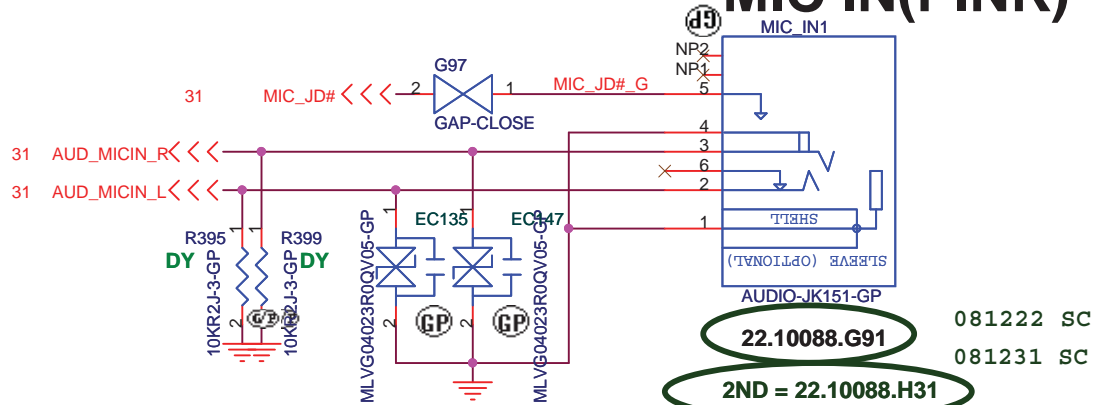
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio AMP for Subwoofer		
Size	Document Number		JM70-PU		Rev
A4					-2
Date:	Friday, March 06, 2009		Sheet	33	of 56

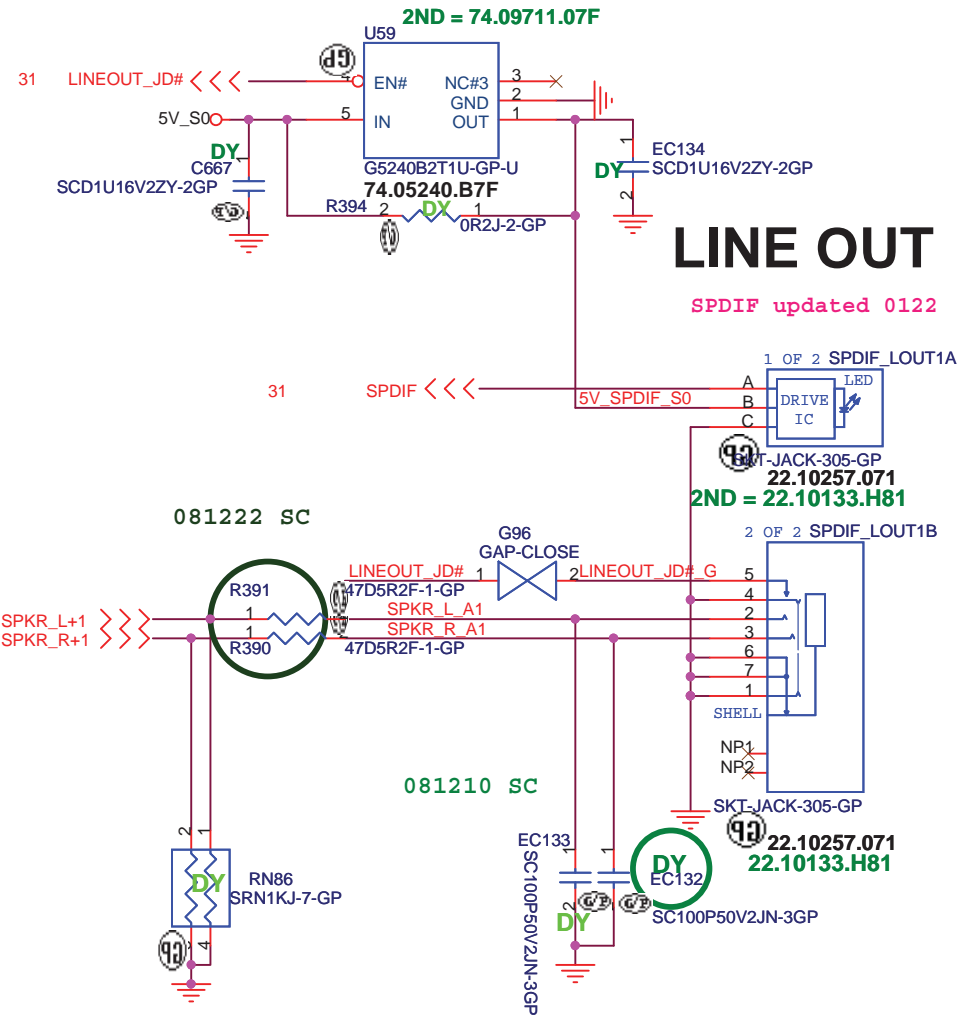
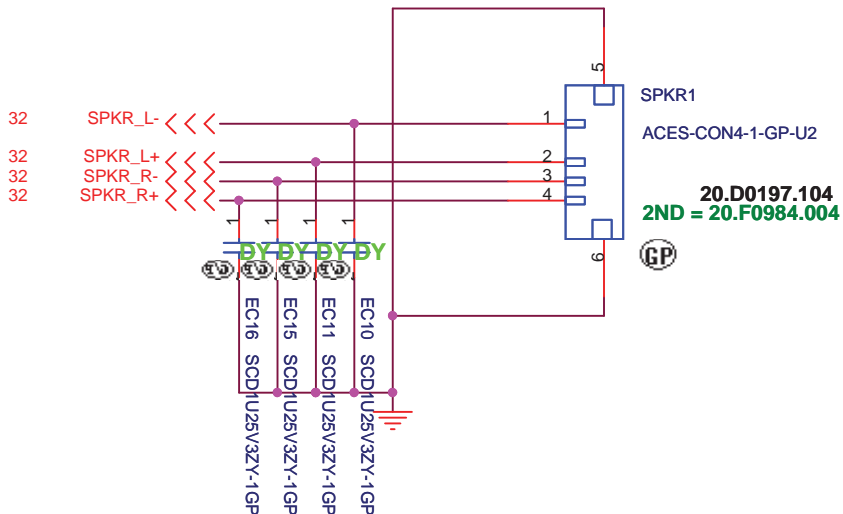
LINE IN(BLUE)



MIC IN(PINK)



REAR Speaker



<Core Design>

緯創資通

Wistron Corporation
215, 22nd St., 4th Fl., Taipei, Taiwan

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AUDIO JACK

Size
A4

Document Number

JM70-PU

Rev
-2

Date: Friday, March 06, 2009

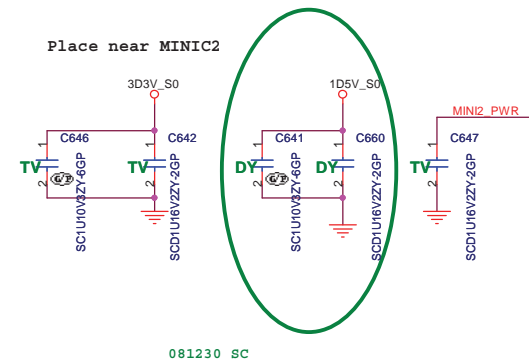
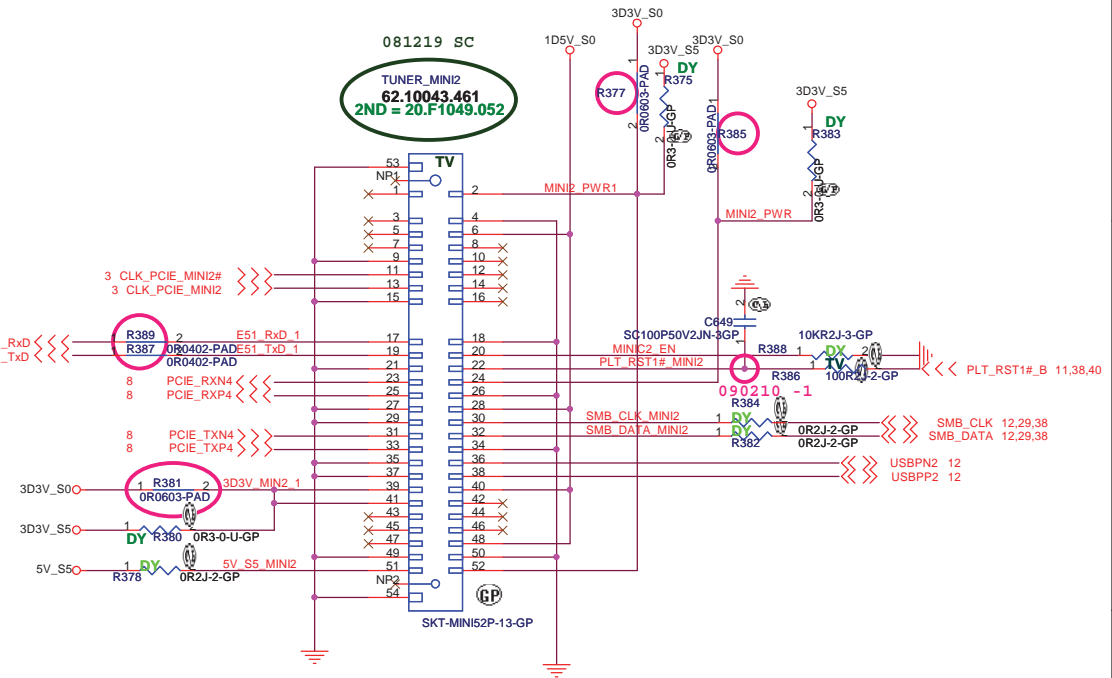
Sheet 34 of 56

The diagram shows a cross-section of a multi-layer PCB with a connector. Four signal traces are shown, each labeled with a signal name, a component value, and a layer reference:

Signal Name	Value	Layer	Component
ACZ_SDATAOUT_MDC	C362	1	SC10P50V2JN-4GP
ACZ_SYNC	C361	1	SC10P50V2JN-4GP
ACZ_RST#	C363	2	SC10P50V2JN-4GP
ACZ_BTCLK_MDC	C365	1	SC10P50V2JN-4GP

The traces are color-coded: ACZ_SDATAOUT_MDC is red, ACZ_SYNC is green, ACZ_RST# is red, and ACZ_BTCLK_MDC is red. The component values are in blue. The layer references are in green. The connector is shown as a vertical stack of pins with a central ground pin.

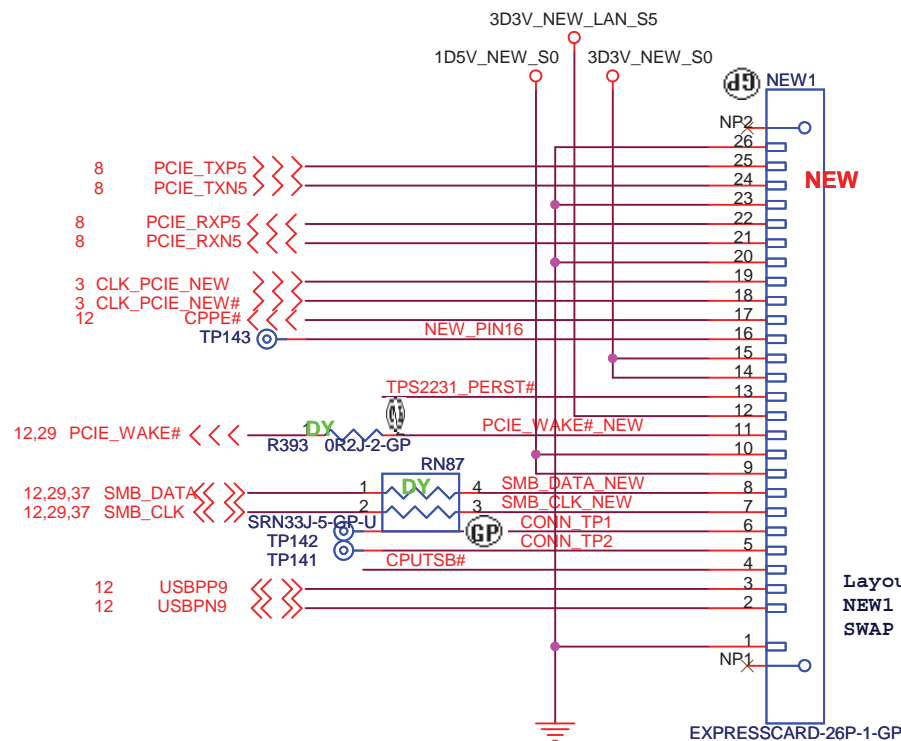
090119 -1



Sheet 37 of 56

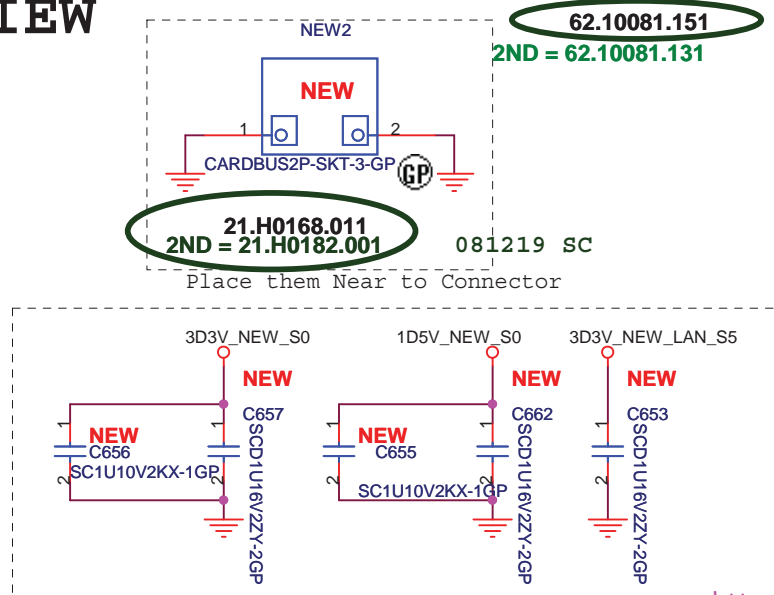
NEWCARD Connector

ENG stage without NEW card function 12/22



TOP VIEW

1
26

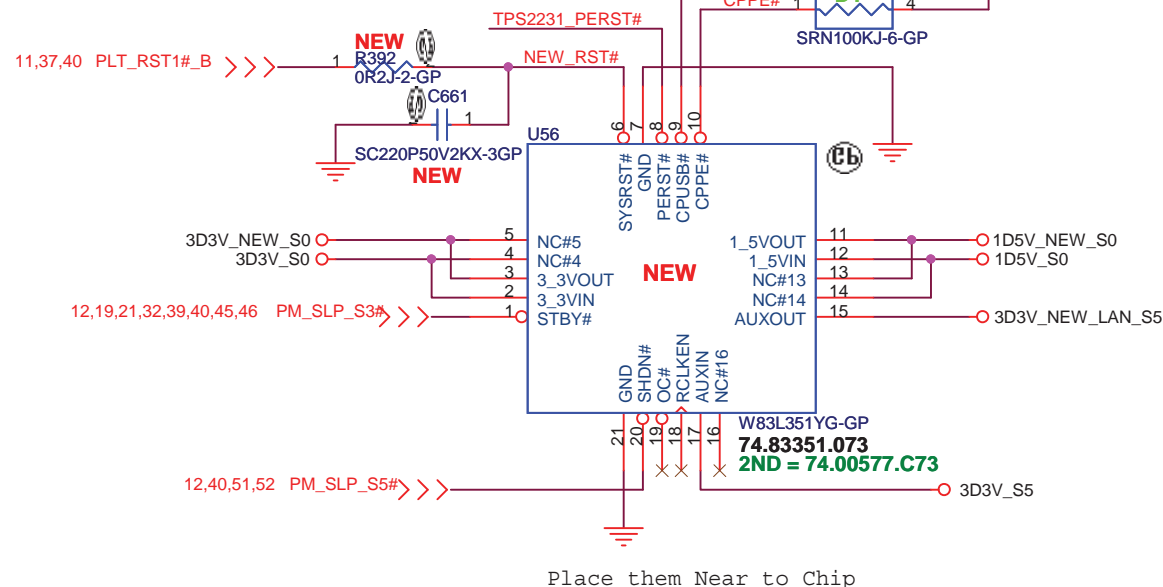


74.00577.C73
new card power switch
GMT cost down solution

081219 SC

62.10081.151
2ND = 62.10081.131

<http://hobi-elektronika.net>



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

NEW CARD

Size

Document Number

A4

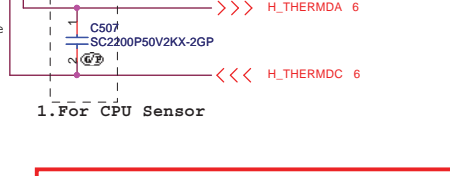
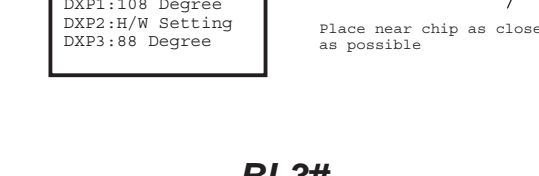
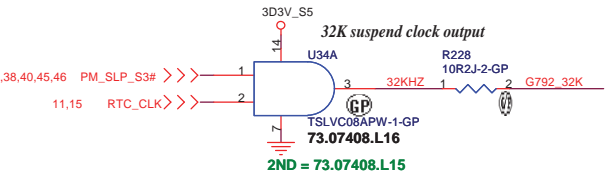
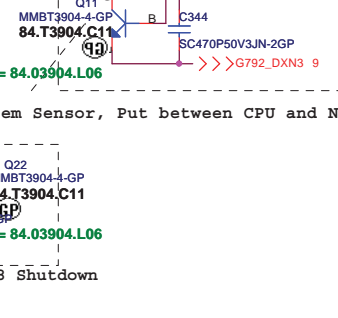
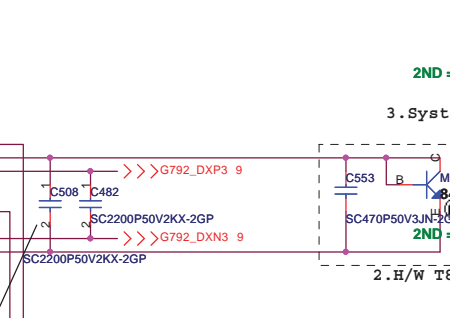
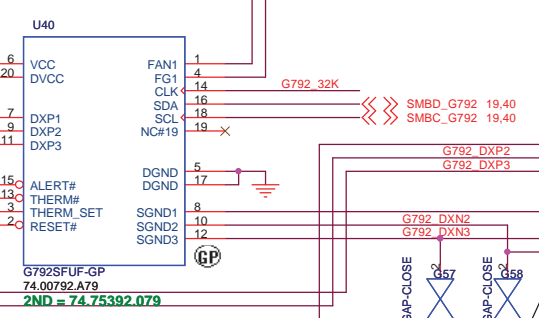
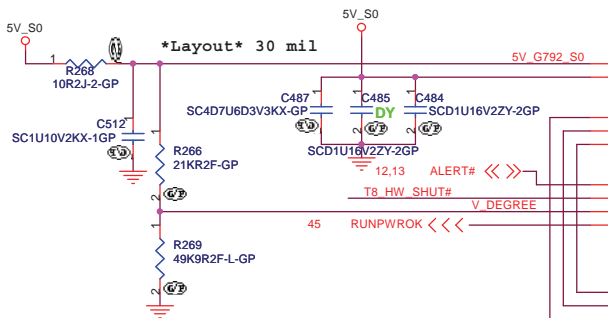
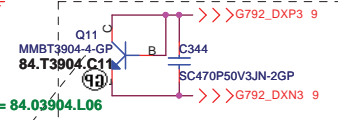
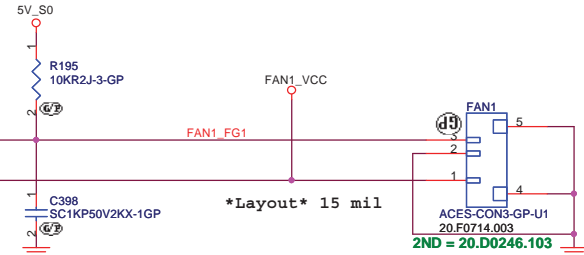
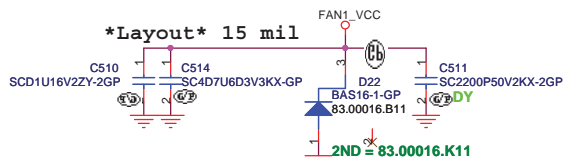
JM70-PU

Rev

-2

Date: Friday, March 06, 2009

Sheet 38 of 56



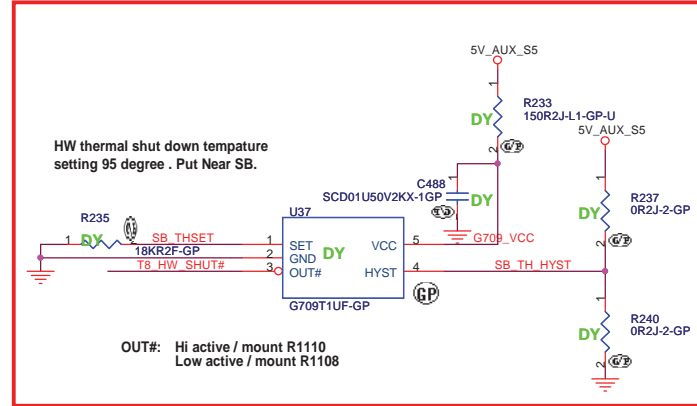
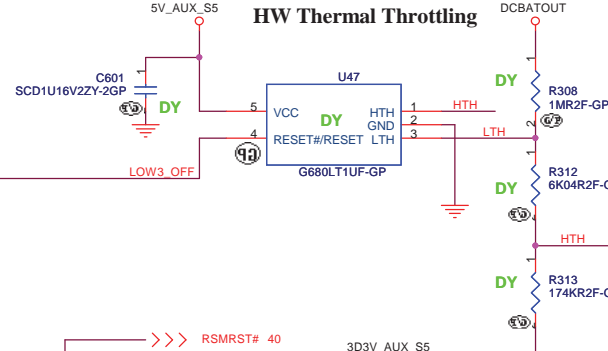
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

1.For CPU Sensor
2.H/W T8 Shutdown
3.System Sensor, Put between CPU and NB.

BL3#

HW Thermal Throttling

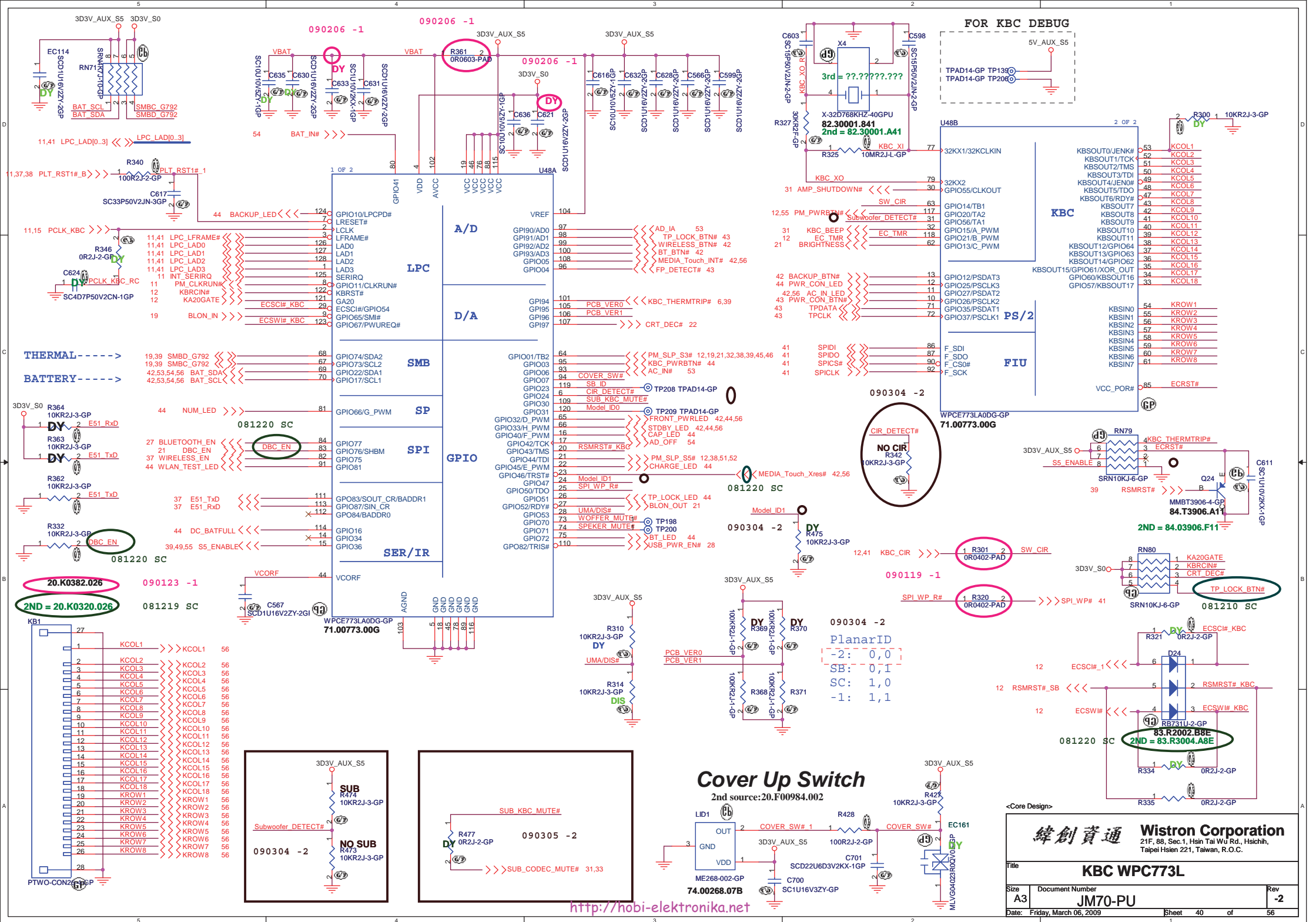


<Core Design>

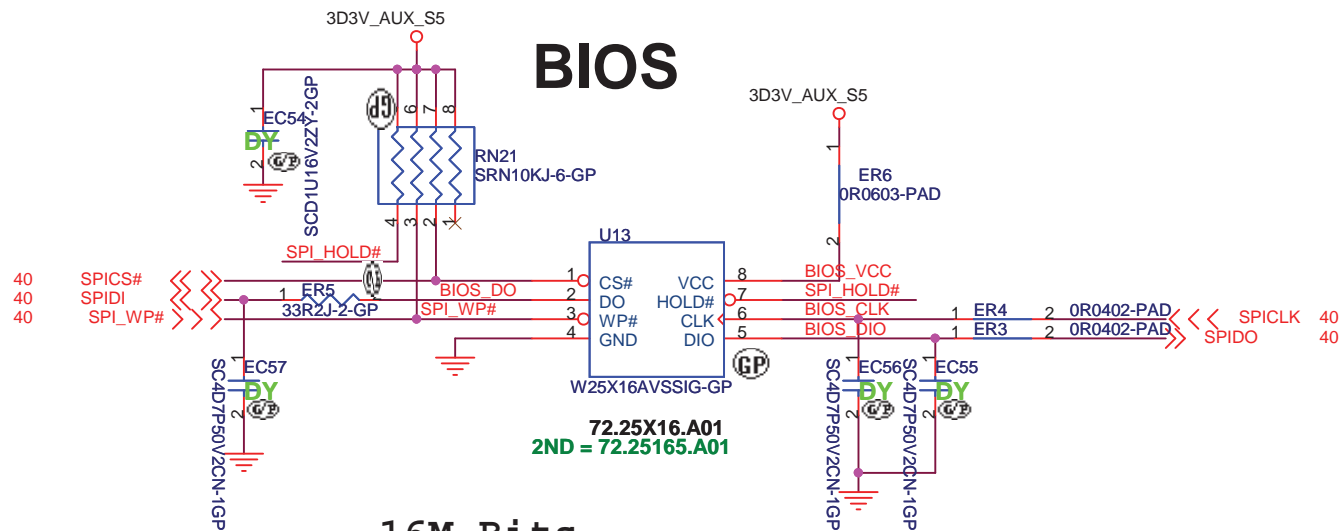
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			G792	
Size	Document Number	JM70-PU		Rev
A3				-2
Date: Friday, March 06, 2009		Sheet 39		of 56

http://www.elektronika.net



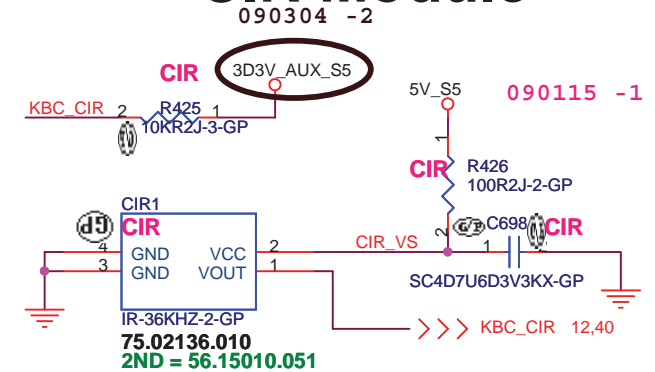
BIOS



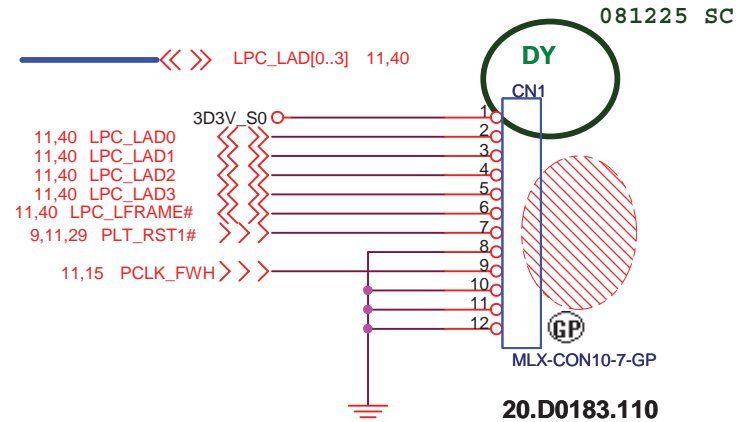
16M Bits

SPI FLASH ROM

CIR Module

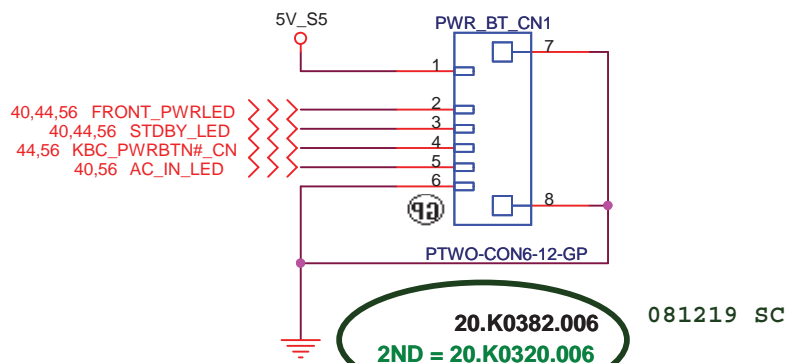
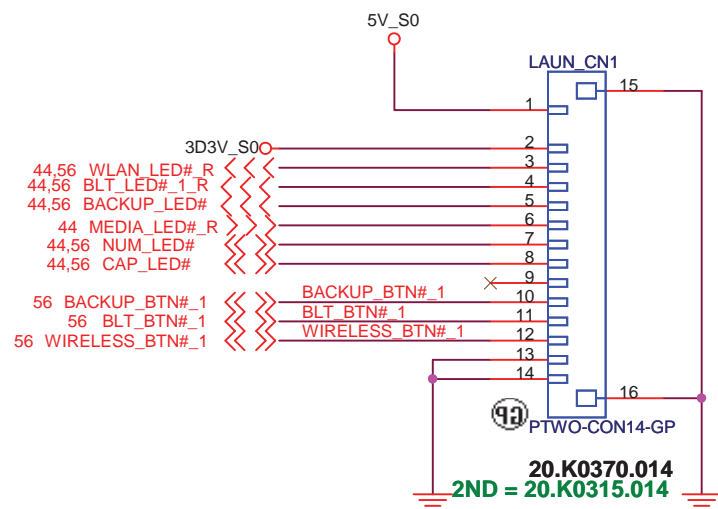
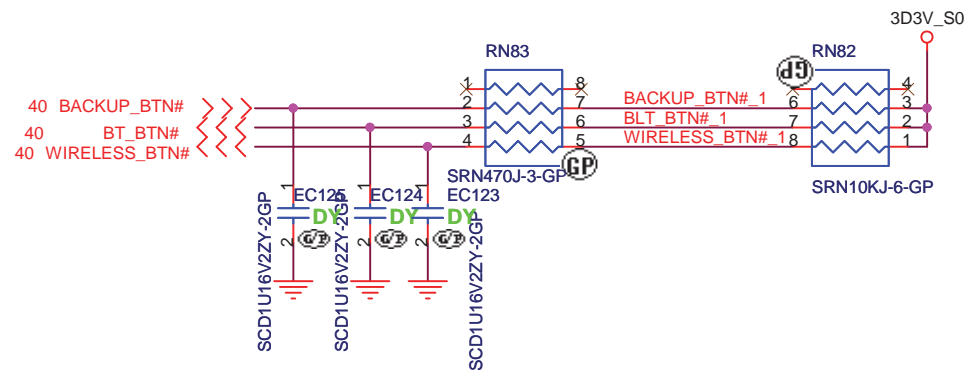


GOLDEN FINGER FOR DEBUG BOARD

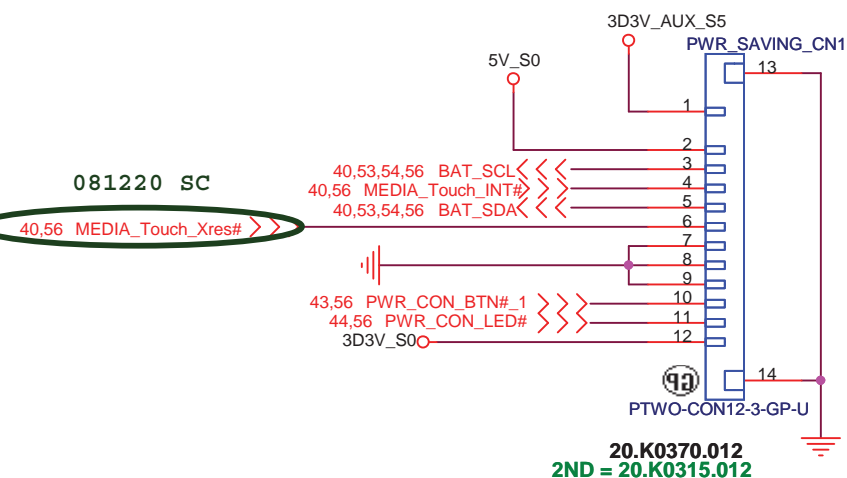
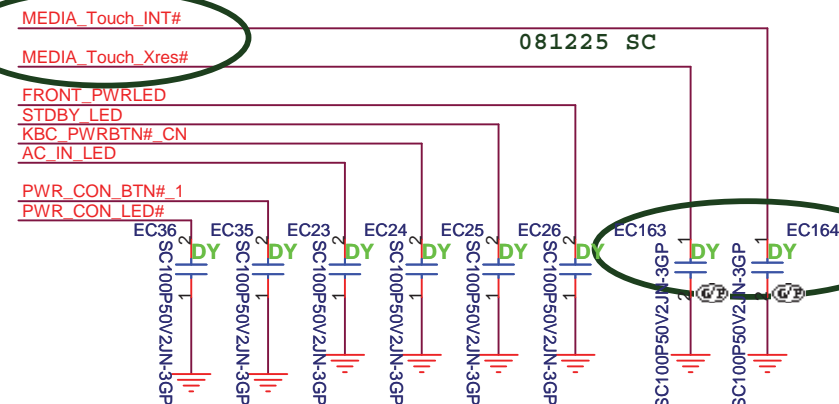


<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
BIOS & CIR		Size	
A4		Document Number	
Date: Friday, March 06, 2009		Rev	
Sheet 41 of 56		JM70-PU	
-2		-2	



LAUNCH



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAUNCH & LID

Size
A4

Document Number

JM70-PU

Rev
-2

Date: Friday, March 06, 2009

Sheet 42 of 56

<http://hobi-elektronika.net>

1 8

12,56 USBPP6

12,56 USBPN6

40 FP_DETECT#

56 TP_LEFT

56 TP_RIGHT

5V_S0

9

1

2

3

4

5

6

7

8

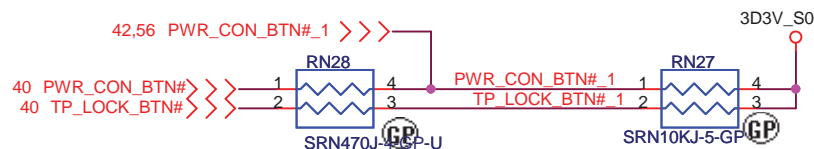
10

PTWO-CON8-6-GP

20.K0381.008

2ND = 20.K0315.008

081219 SC



TP_LOCK1

TP_LOCK_BTN#_1

1 3 5

2 4

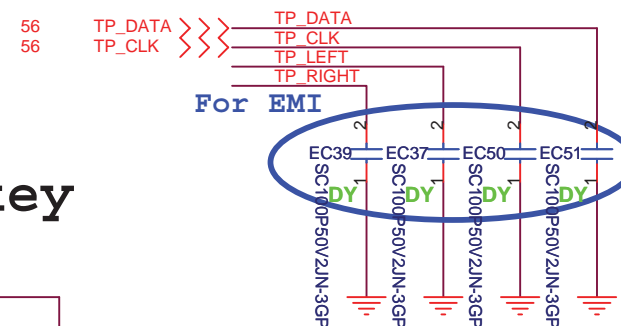
SW-TACT-119-GP (GP)

62.40009.671

2ND = 62.40012.101

The schematic diagram illustrates the electrical connections for the TP1 module. Key components and connections include:

- Power Supply:** A 5V_S0 supply is connected to the module's power pins.
- Resistors:** SRN10KJ-5-GP and SRN33J-5-GP-U are used for signal conditioning.
- Signal Connections:**
 - TP_DATA and TP_CLK signals are connected to pins 2 and 3 of the PTWO-CON6-8-GP connector.
 - TP_RIGHT and TP_LEFT signals are connected to pins 5 and 6 of the same connector.
- Grounding:** A ground connection is shown for the module's common reference.
- Part Identification:** The module is identified by the part number 20.K0322.006, and the connector is labeled PTWO-CON6-8-GP.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A4

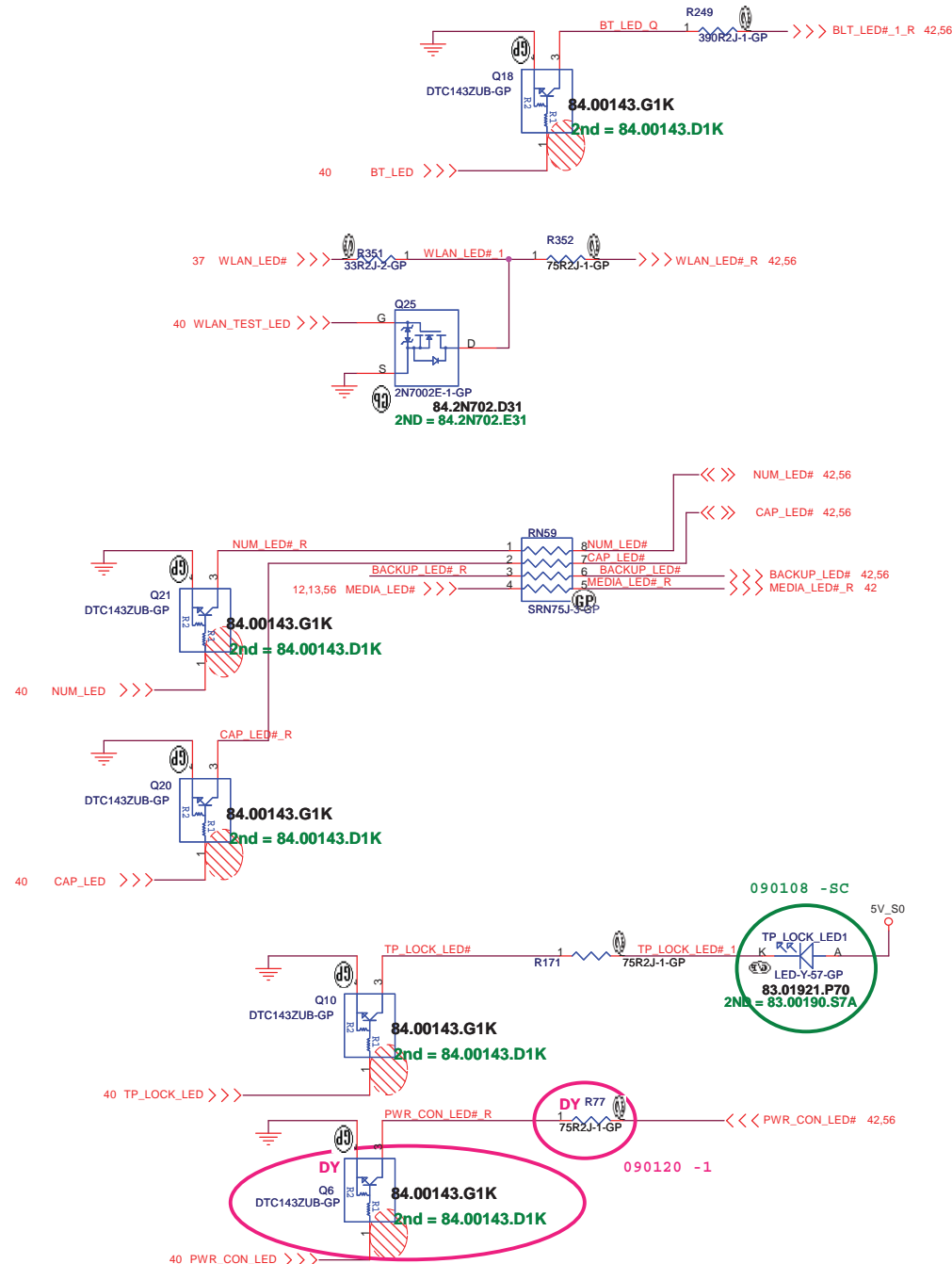
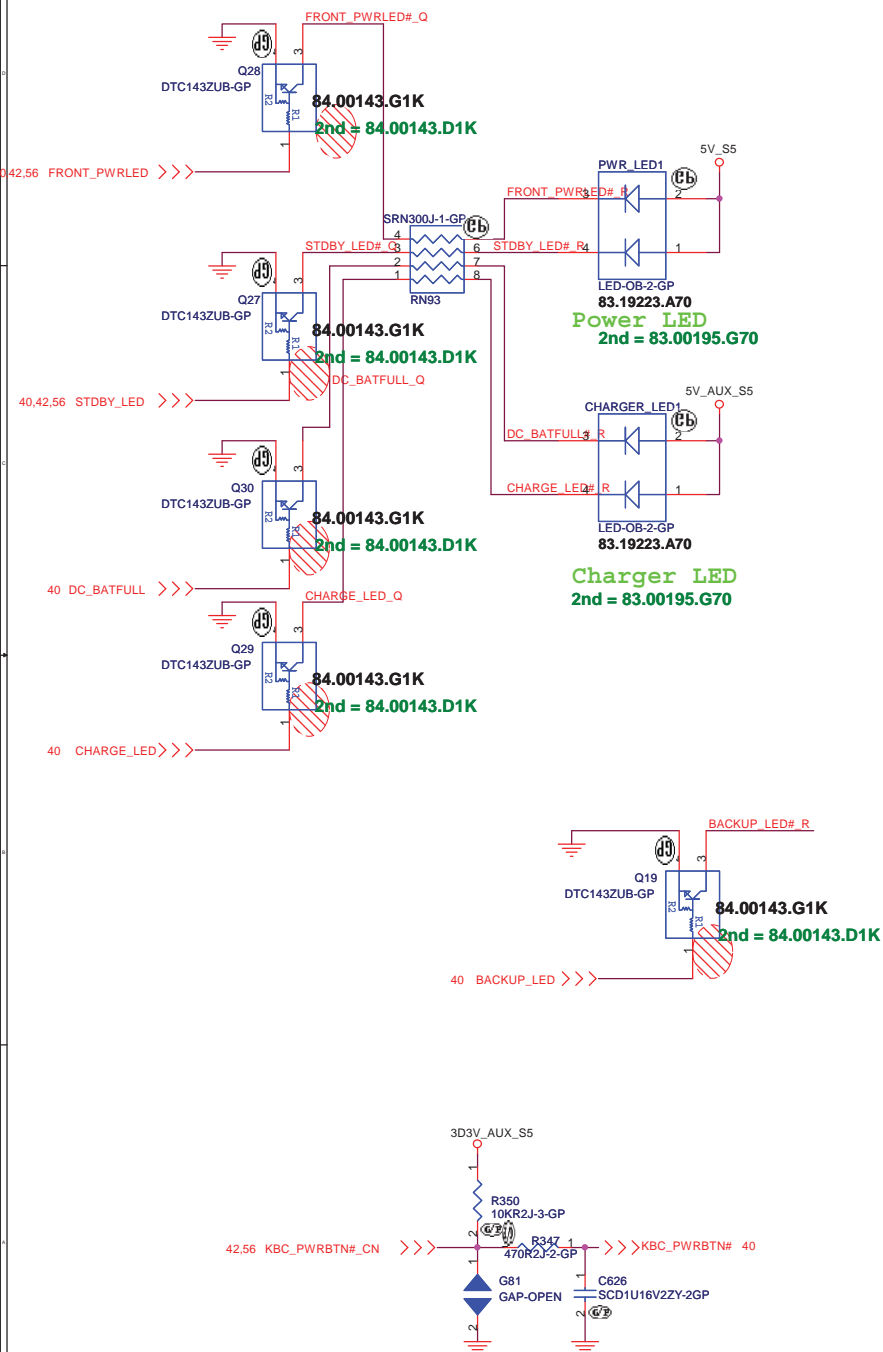
Document Number

Rev	-2
-----	----

Date: Friday, March 06, 2009

Sheet 43 of 56

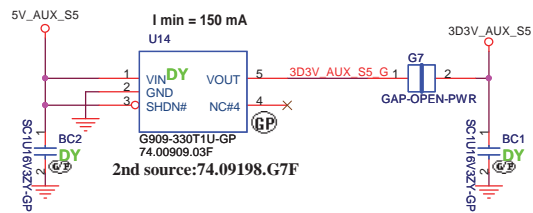
LED



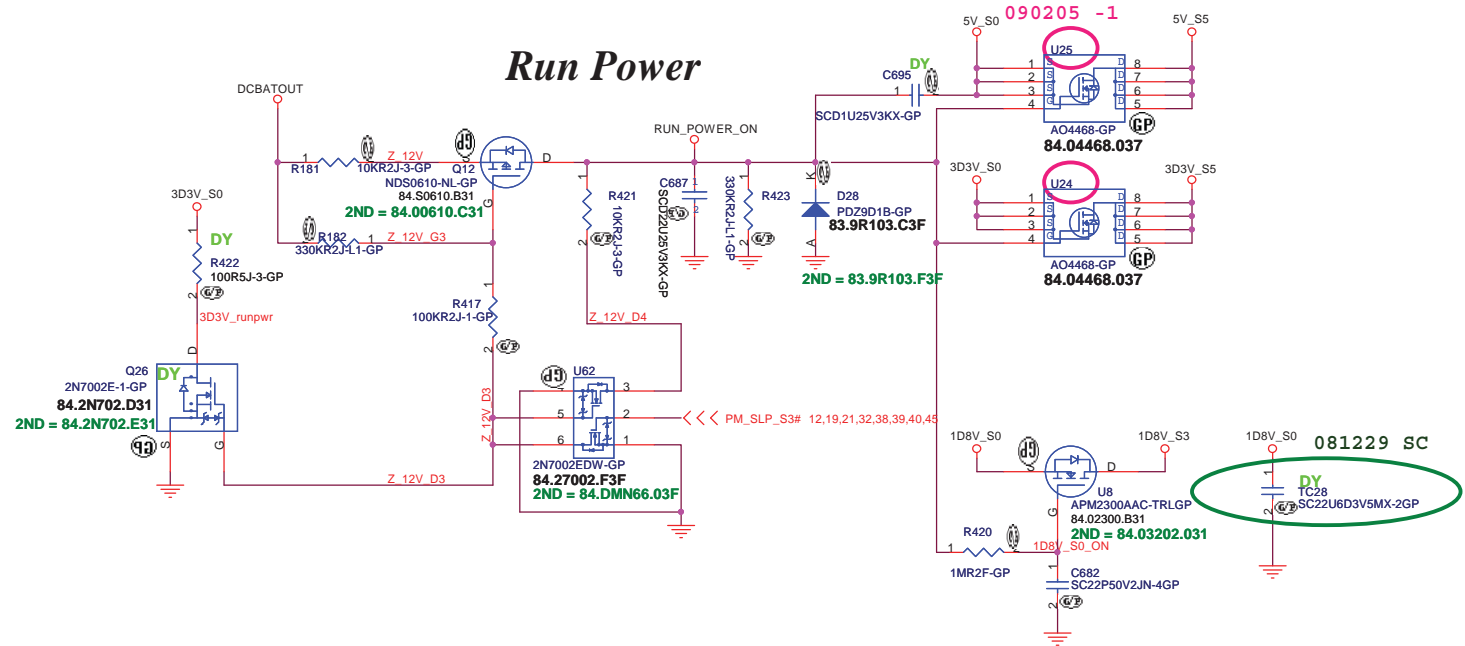


Title			
POWER ON LOGIC			
Size	Document Number	Rev	
A3	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet 45 of	56

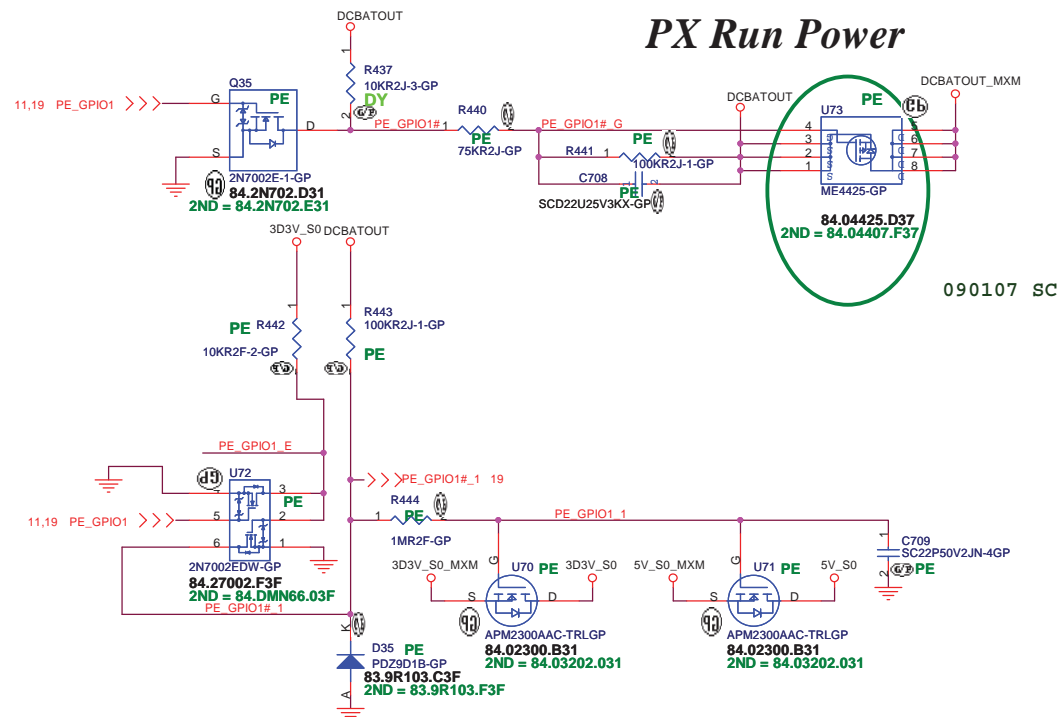
Aux Power 3D3V_AUX_S5



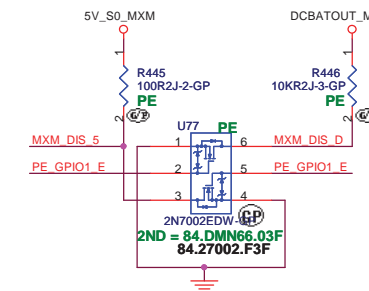
Run Power



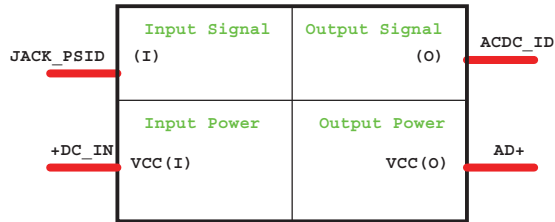
PX Run Power



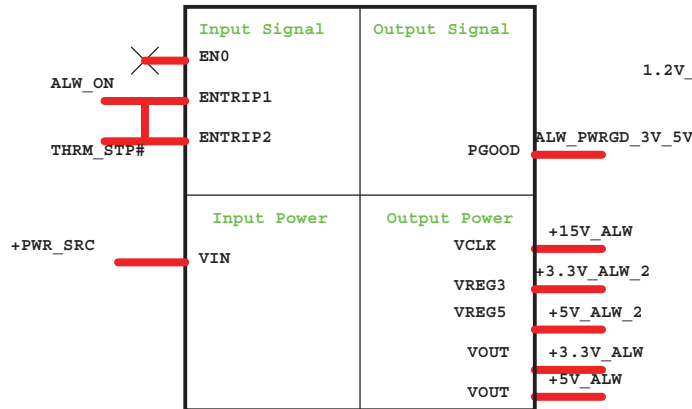
PX Run Power Discharge circuit



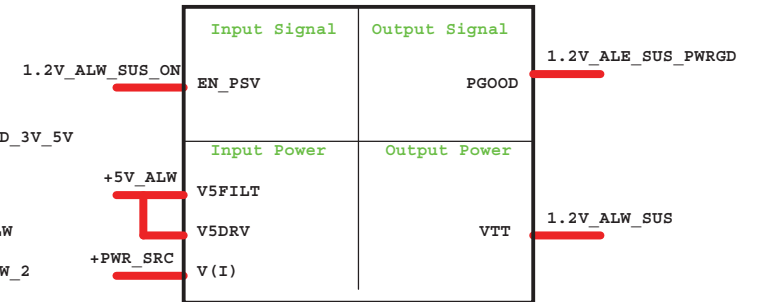
Adapter



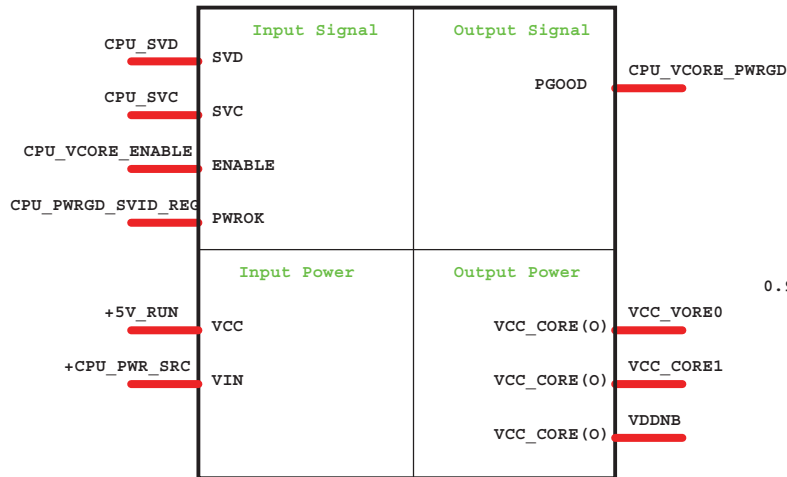
SN0608098



DCDC 1D2V(TPS5117)

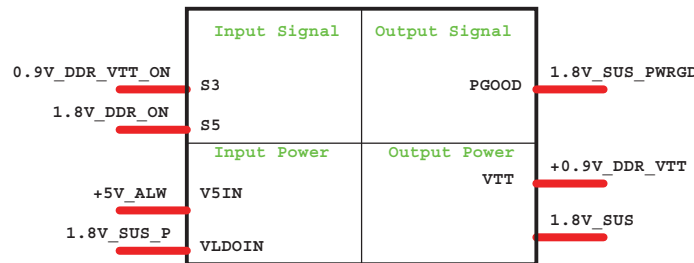


CPU_CORE ISL6265HRTZ

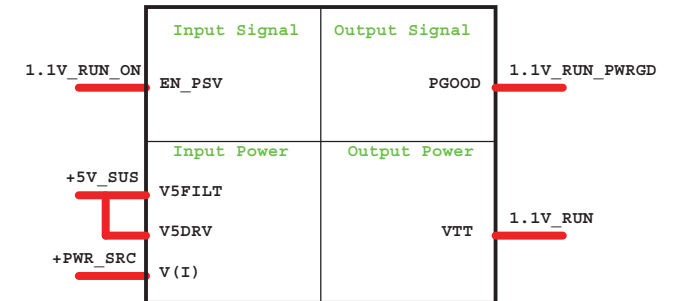


	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	1	1	1
S4	0	0	0	0	0

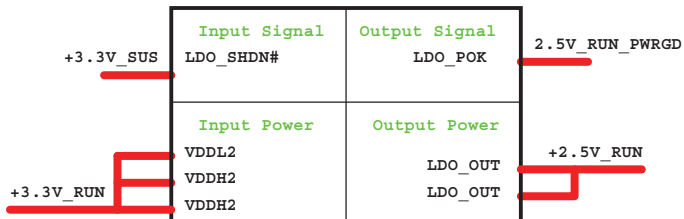
1D8V/0D9V(TPS5116)



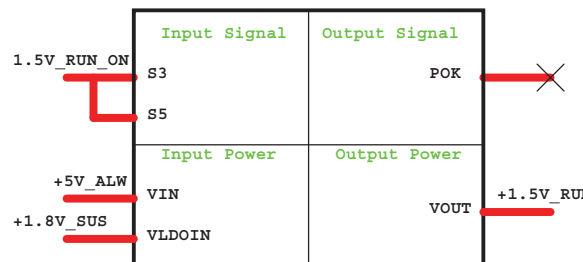
1D1V(TPS5117)



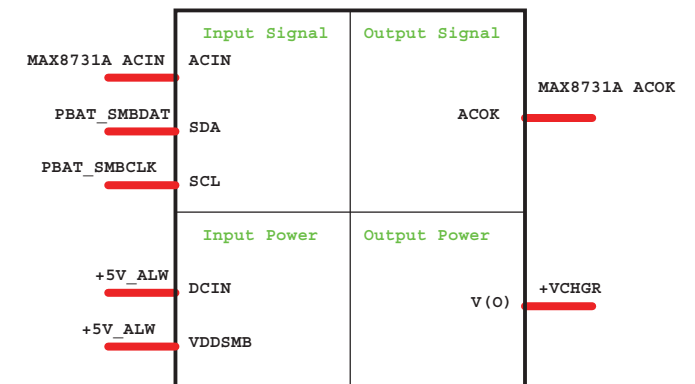
2.5V LDO EMC4002



1.5V LDO



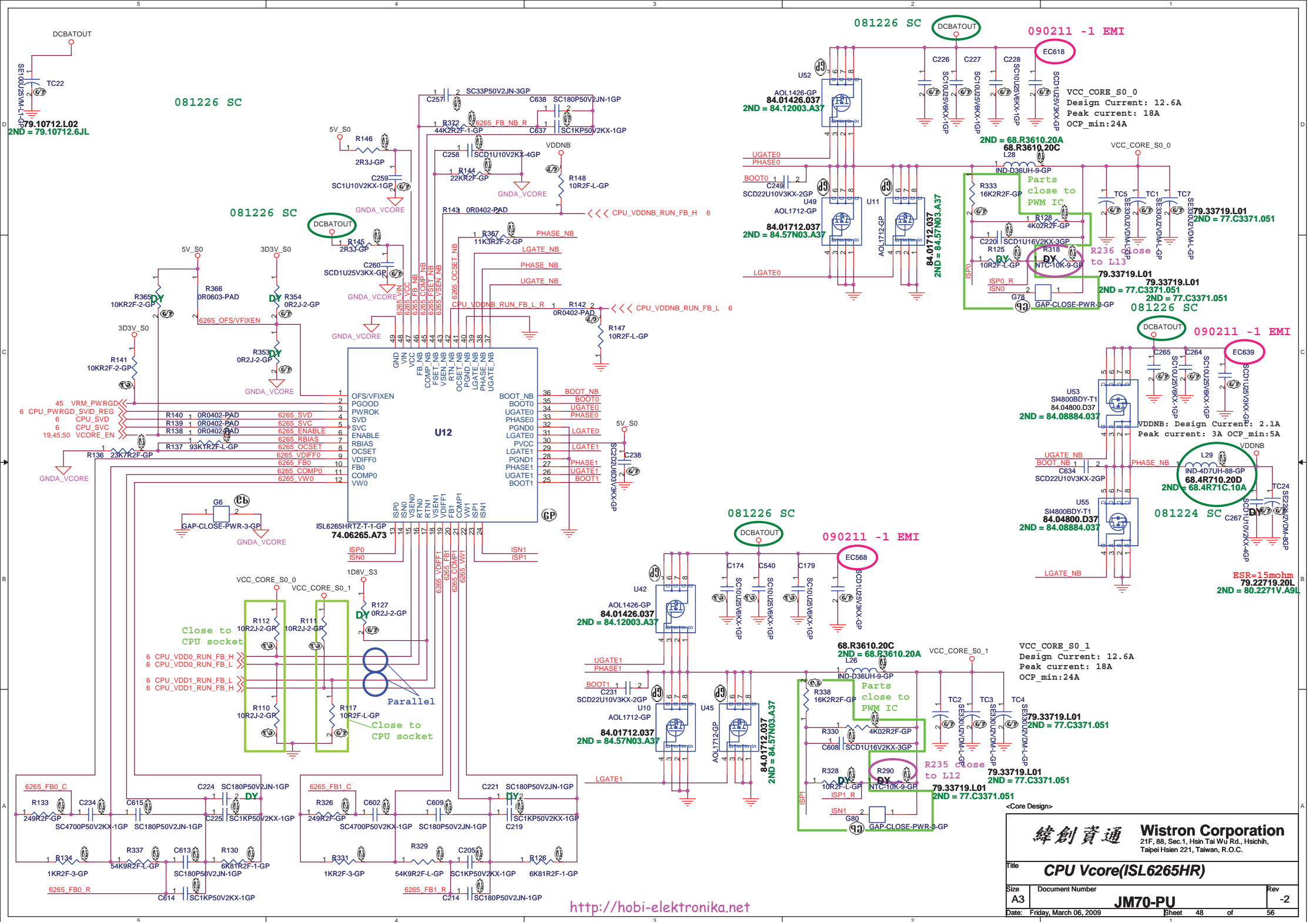
CHARGER BQ24745

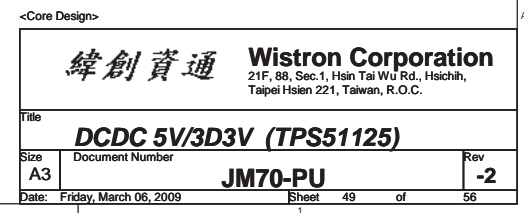


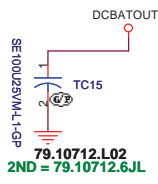
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power Block Diagram		
Size	Document Number	Rev	
A3	JM70-PU	-2	
Date:	Monday, March 02, 2009	Sheet	47 of 56



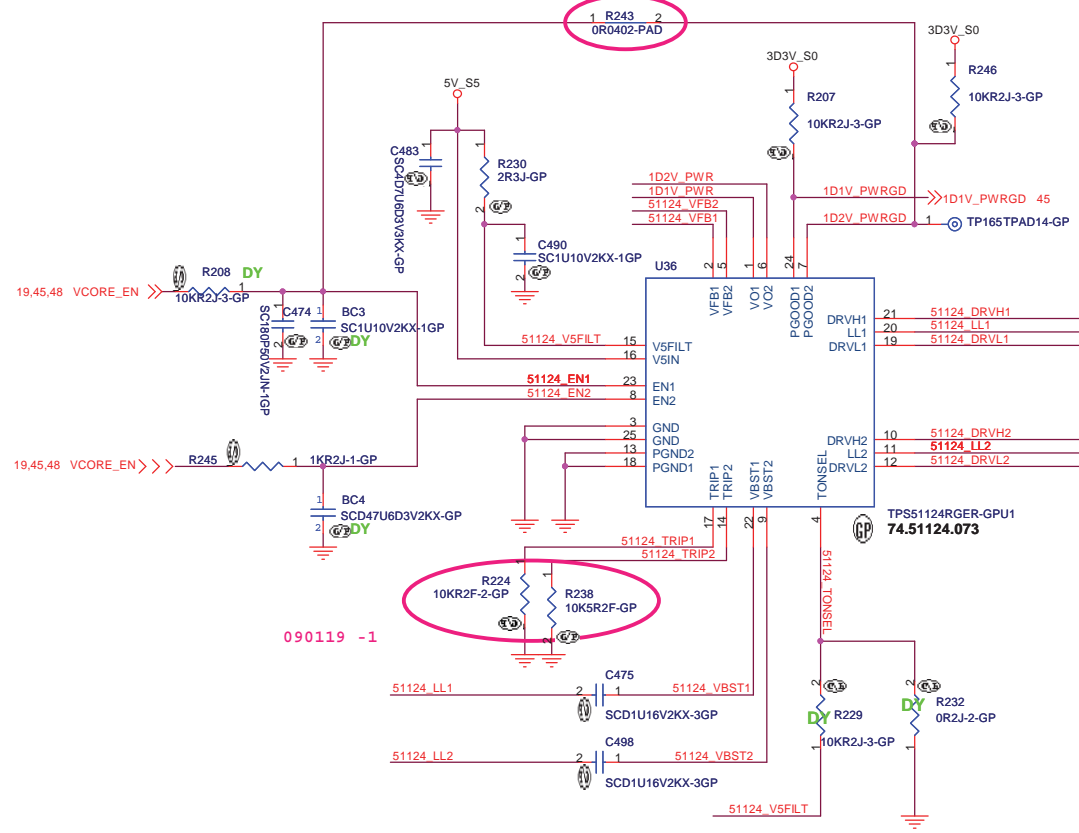




$$V_{trip} (mV) = R_{trip} (Kohm) * I_0 (uA)$$

$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * F)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

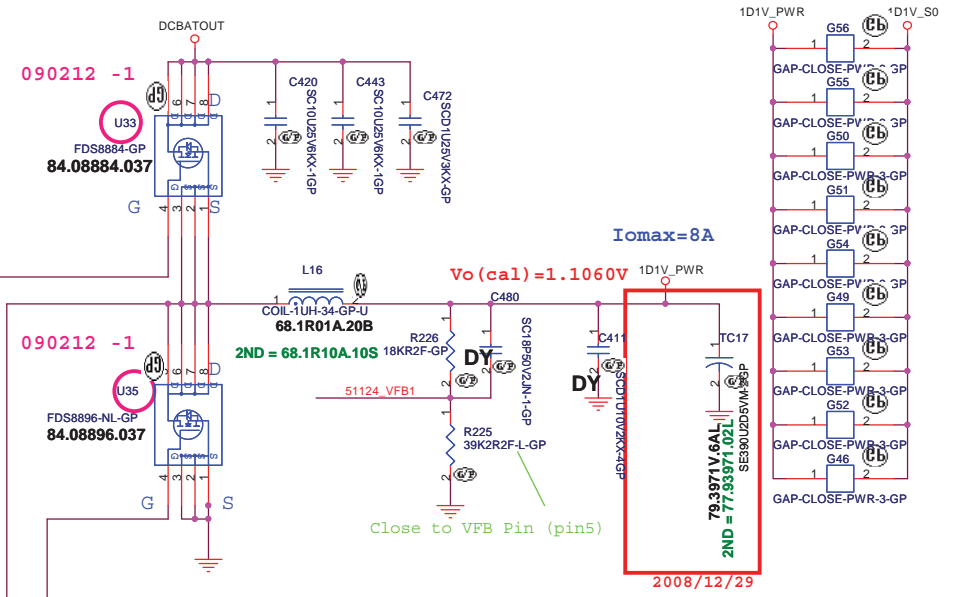
090205 -1



090119 -1

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



090212 -1

090213 -1

090213 -1

20080307_Modify by
Brian
ACOUSTIC NIOSE

Iomax=8A

$V_o (cal) = 1.1060V$

DY

TC17

79.3971V.6AL
2ND = 77.93971.02L

2008/12/29

1D2V Iomax=5A
OCP>10A

DY

TC21

79.3971V.6AL
2ND = 77.93971.02L

2008/12/29

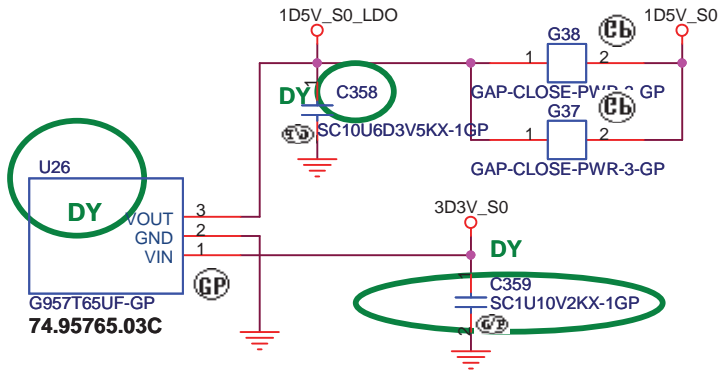
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			TPS51124 1D1V 1D2V
Size	Document Number	Rev	
A3	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	50 of 56

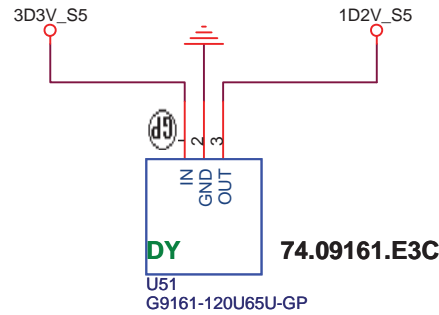
G957

1D5V_S0
Iomax=1A

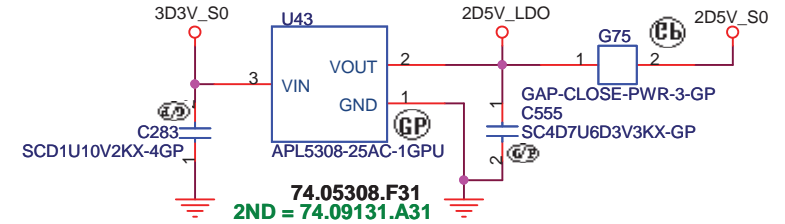


081230 SC

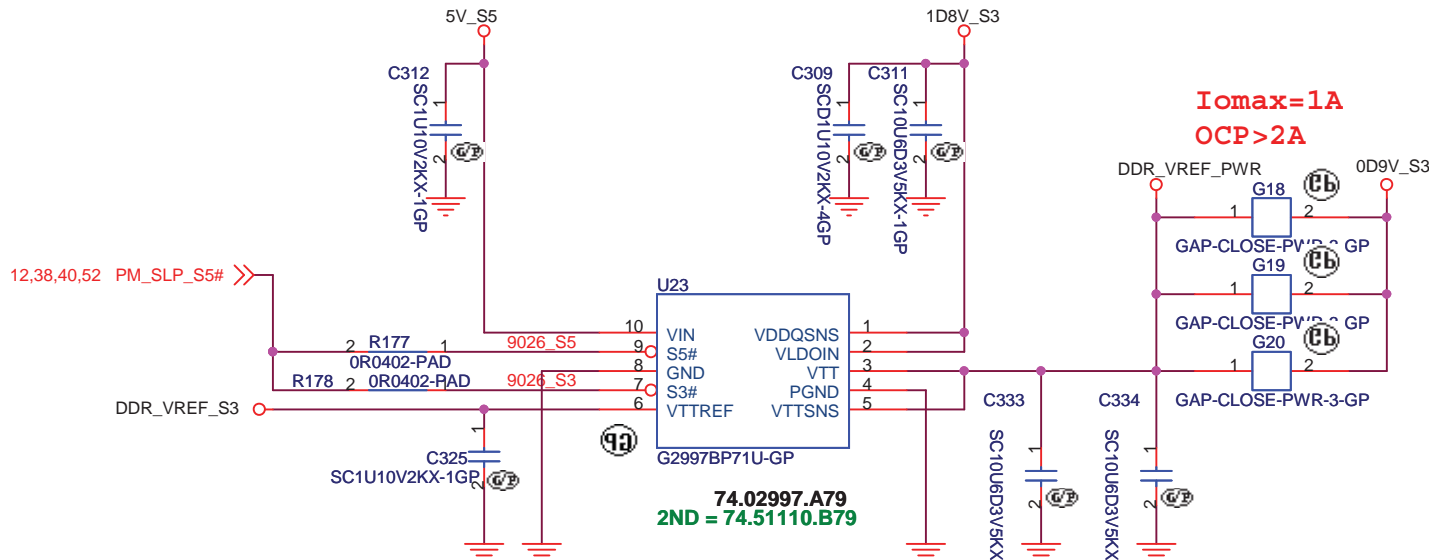
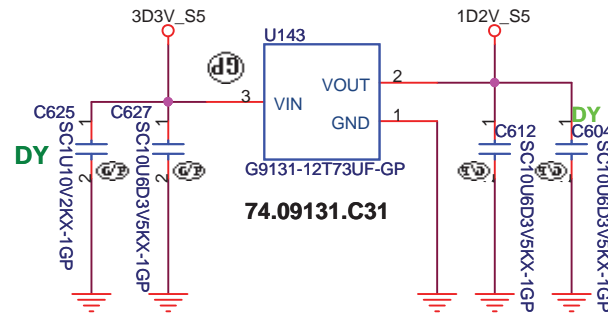
1D2V_S5
Iomax=400mA



2D5V_S0
Iomax=0.3A 2D5V/300mA



Place near to SB700



Iomax=1A
OCP>2A

<Core Design>

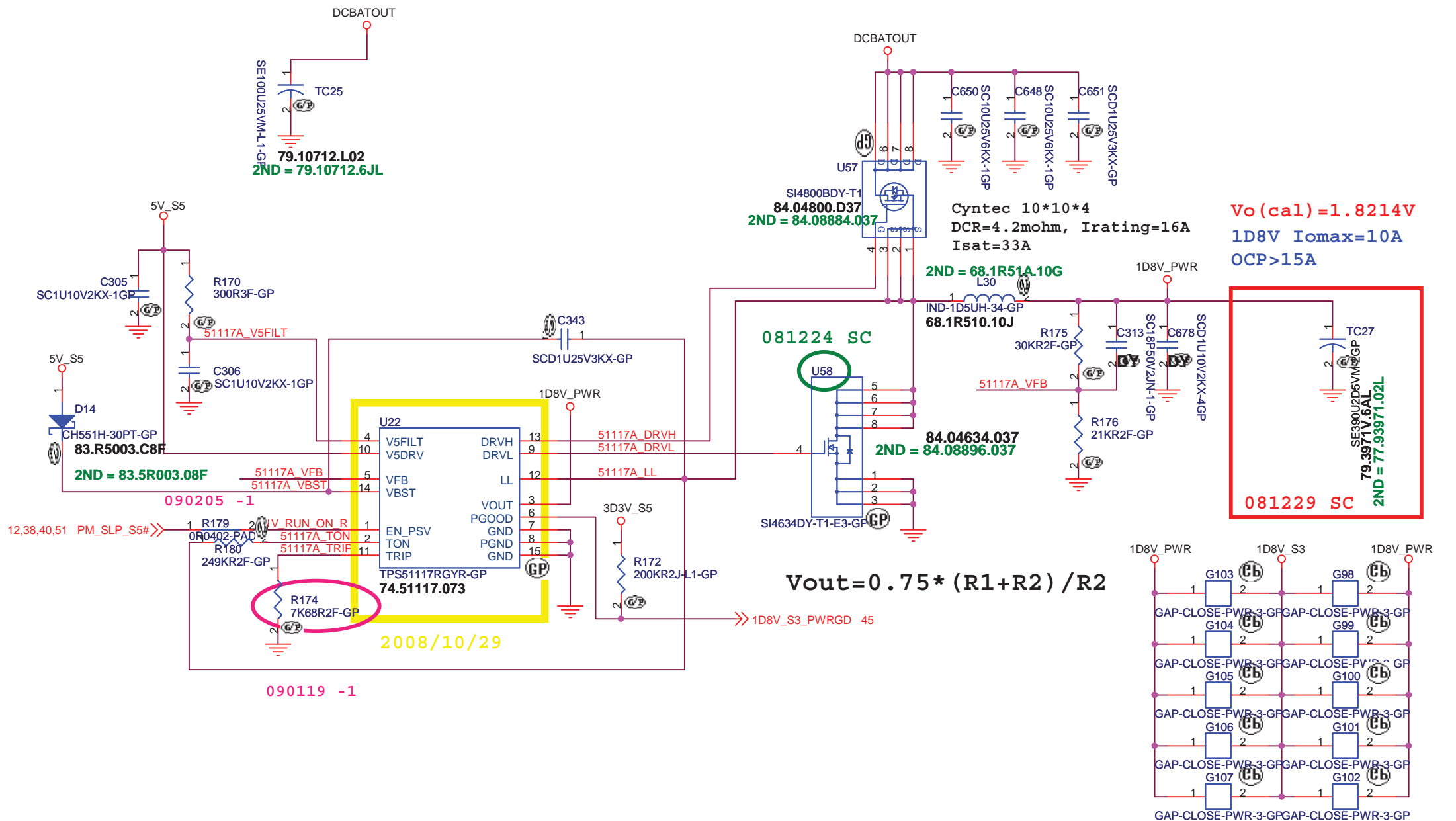
緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
0D9V&2D5V&1D25V&1D5V		
Size	Document Number	Rev
A4	JM70-PU	-2
Date:	Friday, March 06, 2009	Sheet 51 of 56

<http://hobi-elektronika.net>



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

1D8V(TPS5117)

Size

A4

Document Number

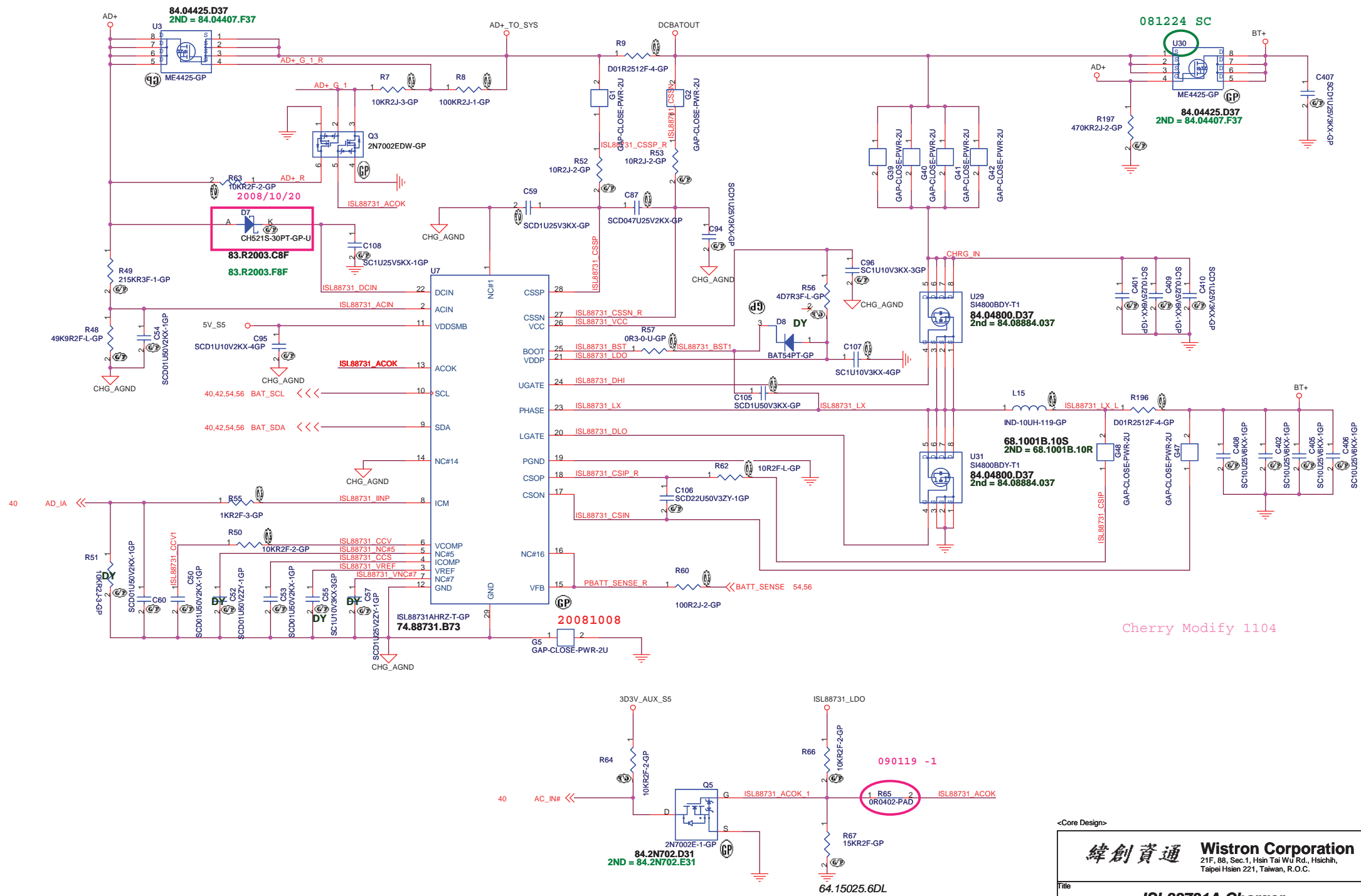
JM70-PU

Rev

-2

Date: Friday, March 06, 2009

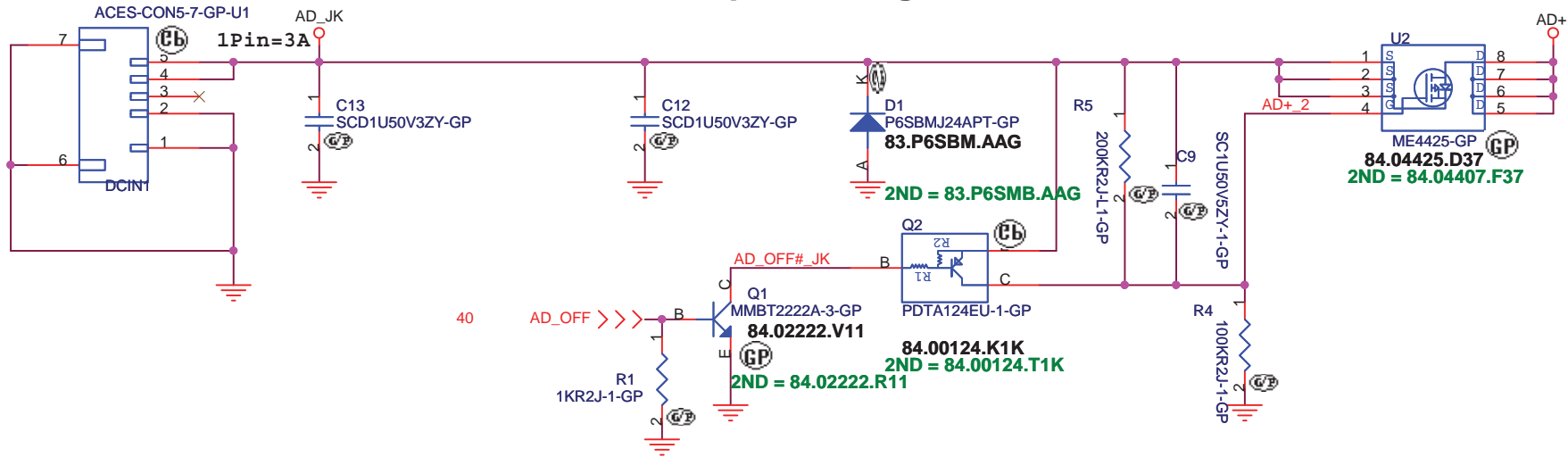
Sheet 52 of 56



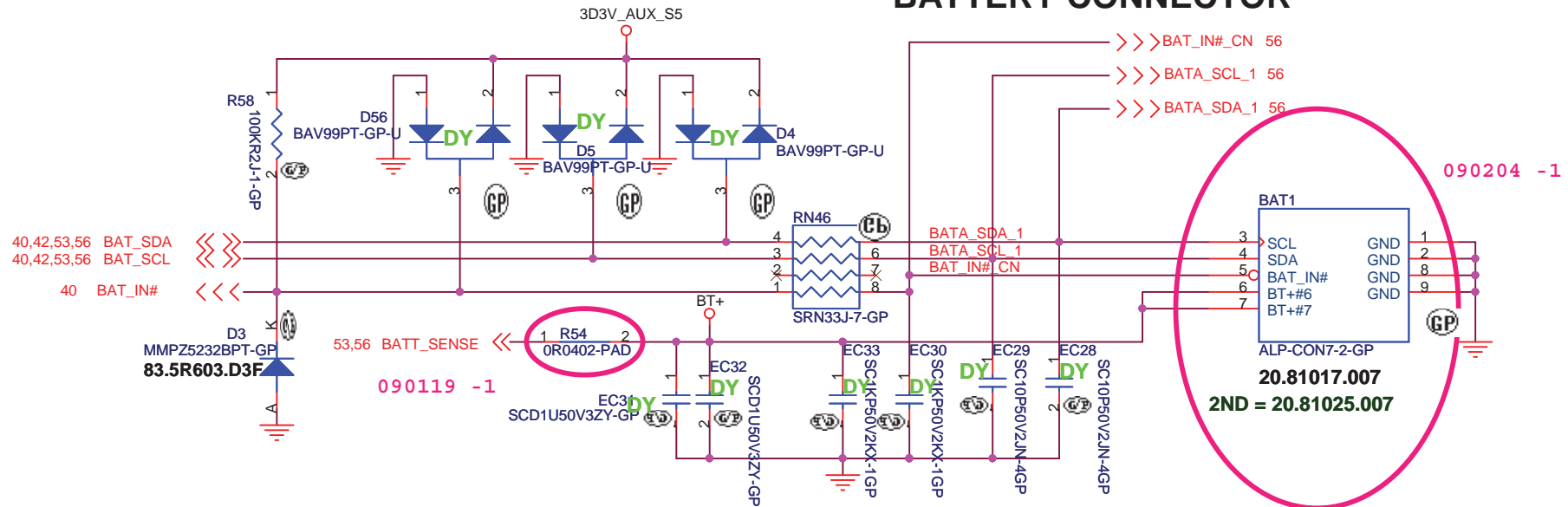
20.F1002.005

2ND = 20.F1170.005

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

A4

Document Number

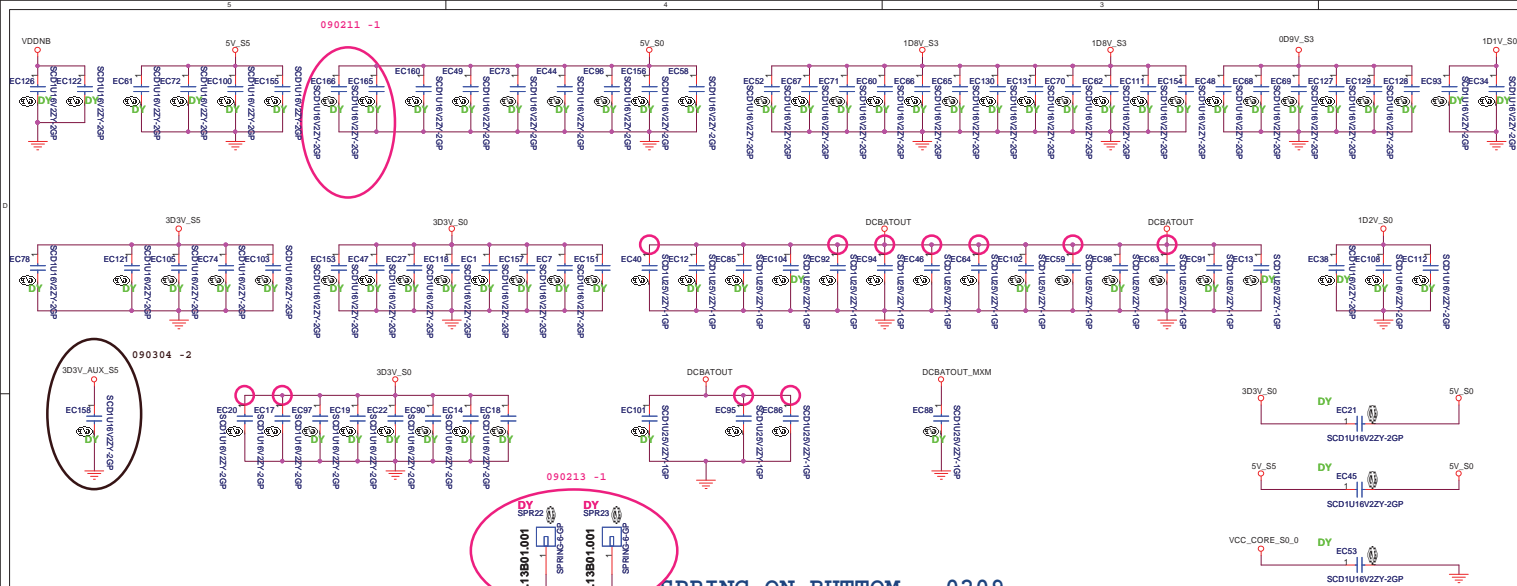
JM70-PU

Rev

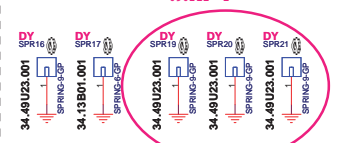
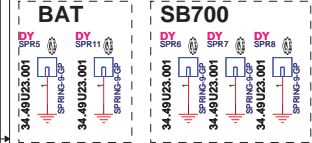
-2

Date: Friday, March 06, 2009

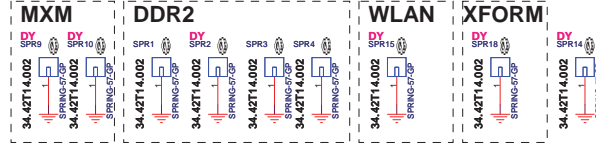
Sheet 54 of 56



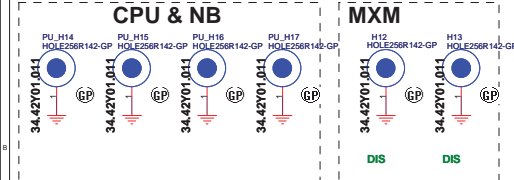
SPRING ON TOP ~ 0209
34.49U23.001 + 34.13B01.001



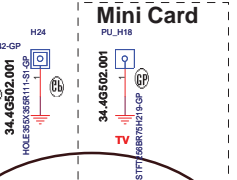
SPRING ON BOTTOM ~ 0209
34.42T14.002



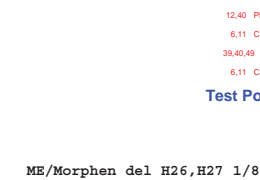
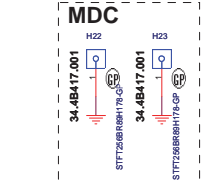
STAND OFF ON BOTTOM ~ 0210



090302 -2



STAND OFF ON TOP ~ 0209



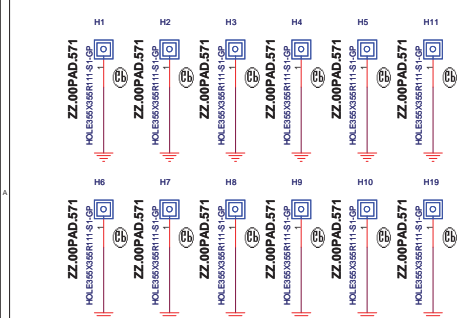
Check test point

- 303V_S0 ○ TP213 TPAD14-GP
- 303V_AUX_S5 ○ TP215 TPAD14-GP
- 303V_S5 ○ TP212 TPAD14-GP
- 5V_S5 ○ TP211 TPAD14-GP
- 12.40_PML_PWRBTN <<< TP176 TPAD14-GP
- 6.11 CPU_PWRGD <<< TP189 TPAD14-GP
- 39.40.49_SS_ENABLE <<< TP207 TPAD14-GP
- 6.11 CPU_LDT_RST <<< TP195 TPAD14-GP

Test Point放在Dimm Door打開可量測處

ME/Morphen del H25 2/10
& recover H25 3/2
& Add H28 3/5

Hall updated -1118



ME/Morphen del H26,H27 1/8

